DATA TRANSLATION

DT2781
DT2785

USER MANUAL

MP MASTER
MA25760

Document UM-00068-4
(Ref. DTI-UM-DT2781-4)

User Manual

for

DT2781
DT2785

DEC DUAL HEIGHT

ANALOG I/O SYSTEM

For LSI-11, LSI-11/2, LSI-11/23

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Corrigenda for the DT2781/DT2785 User Manual (UM-00068-4)

for DTAXV11-C and DTADV11-C users

July, 1985

For the most part, the DT2781 User Manual can be used as it is. The major differences include:

1. Factory shipment on the DTAXV11-C and DTADV11-C is offset binary instead of two's complement for the A/D.

2. Factory shipment of offset binary for the DACs on the DTAXV11-C.

3. Programmable gain (1, 2, 4, and 8) is standard, not an option.

4. Unlike the DTAXV11-C and DT2781, the DTADV11-C does not have any analog output (DAC) circuitry.

5. The connector (J1) output is different for the ADV11-C. There are no DAC signals on the connector. Pins 23, 24, 25, and 26 are "no connection" on the J1 connector.

6. The specifications for the DTAXV11-C and DTADV11-C that differ from the specifications for the DT2781 include:

   a) The power requirement is +5 Volts (±5%) @2.0A

   b) Input Impedance, Power Off is 1 kilohm in series with a diode

   c) Input bias current is 20nA max

   d) Inputs are current-limited and protected to ±30 volts without damage (power on)

   e) Input noise is less than 0.2 microvolts rms

   f) System throughput* is 25 microseconds from starting A/D conversion to setting the A/D DONE bit; or 25K channel samples per second**.

---

* Throughput on a programmed I/O board does not take into account bus activity.

** Channel settling time is 15 microseconds for a total time of 40 microseconds.

The DTAXV11-C and DTADV11-C can be tested with the DT2781 (SP0031) diagnostics with the following conditions:

1. Enter "MODEL DT2781" when prompted for a model number.

2. Unless changed from factory shipment, answer "N" for two's complement.

3. For the DTADV11-C, the DAC tests will not produce an output (no error will be returned). Tables CORR-1 and CORR-2 show the DAC tests for versions 1.03 and 1.06 of the SP0031 diagnostics.

TABLE CORR-1: VERSION 1.03 DAC TESTS

VERSION 1.03 TEST NUMBER AND NAME
13 - A/D IN TO D/A OUT 14 - D/A RAMPS 15 - D/A CALIBRATION 16 - D/A SQUARE WAVES 17 - D/A OUT TO A/D IN

TABLE CORR-2: VERSION 1.06 DAC TESTS

VERSION 1.06 TEST NUMBER AND NAME
17 - A/D IN TO D/A OUT 20 - D/A RAMPS 21 - D/A CALIBRATION 22 - D/A SQUARE WAVES 23 - D/A OUT TO A/D IN

MAXIMUM INPUT VOLTAGE WITHOUT DAMAGE FOR DATA TRANSLATION A/D CONVERSION BOARDS

The multiplexers used in Data Translation A/D converters can be damaged if the input voltages applied to the A/D input connections exceed certain threshold values.

Figure 1 contains the maximum voltage values, both normal mode and common mode, which various Data Translation A/D converter modules can tolerate (Common mode voltages apply only to differential modules, or modules (like the DT5712) jumpered to operate in differential mode.). Note that the maximum voltage which these inputs can tolerate is greatly reduced when the modules are powered down.

Users of Data Translation analog input boards should note the model number of the A/D converter module or input expander module used on their board and check the "MAX VOLTAGE W/O DAMAGE" values listed in Figure 1. The A/D converter or expander module is housed in a 3" long by 4.6" high black steel package. Each is labelled with a model number on the top of the module housing.

WARNING

Applying input voltages to a Data Translation A/D board in excess of the values specified in Figure 1 for the module used on that board will cause irreparable damage to the module, and will void the warranty on the board.

MAXIMUM INPUT VOLTAGE VALUES FOR DATA TRANSLATION MODULES

A/D MODULE	MAX VOLTAGE W/O DAMAGE (POWER ON)	MAX VOLTAGE W/O DAMAGE (POWER OFF)
DT5701	+/-16V	+/-1V
DT5702	+/-35V	+/-20V
DT5703/03EX	+/-15V*	+/-250V
DT5704/04EX	+/-31V	+/-16V
DT5710/10A	+/-16V	+/-1V
DT5712/02EX	+/-35V	+/-20V
DT5714/16	+/-16V	+/-1V
DT16EX/48EX	+/-16V	+/-1V
DT5722	+/-16V	+/-1V

*Common mode voltages can be +/-250V without damage. Differential voltage an be 100V for 10ms maximum.

FIGURE 1

NOTES ON USING DATA TRANSLATION A/D BOARDS:

When making connections to Data Translation A/D boards, a few matters should be considered to assure proper operation. PLEASE READ THE FOLLOWING COMMENTS BEFORE OPERATING THE BOARD.

UNUSED ANALOG INPUTS

All unused analog input channels should be connected to Analog Common. Failure to do this can result in inaccurate A/D conversions on channels adjacent to the unused channels.

DIFFERENTIAL INPUTS

The low end of each differential input must be referenced to Analog Common. This can be done by connecting a 10 kilohm resistor between the low end of each differential input and Analog Common.

If all inputs share a common ground, a single 1 kilohm resistor can be connected between the input signal common and the board Analog Common.

SINGLE-ENDED AND PSEUDO-DIFFERENTIAL INPUTS

When single-ended or pseudo-differential inputs are used, you must always reference Amp Low to Analog Common. This can be accomplished by connecting Amp Low to Analog Ground at the point of connection of the user signal.

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CHAPTER 1

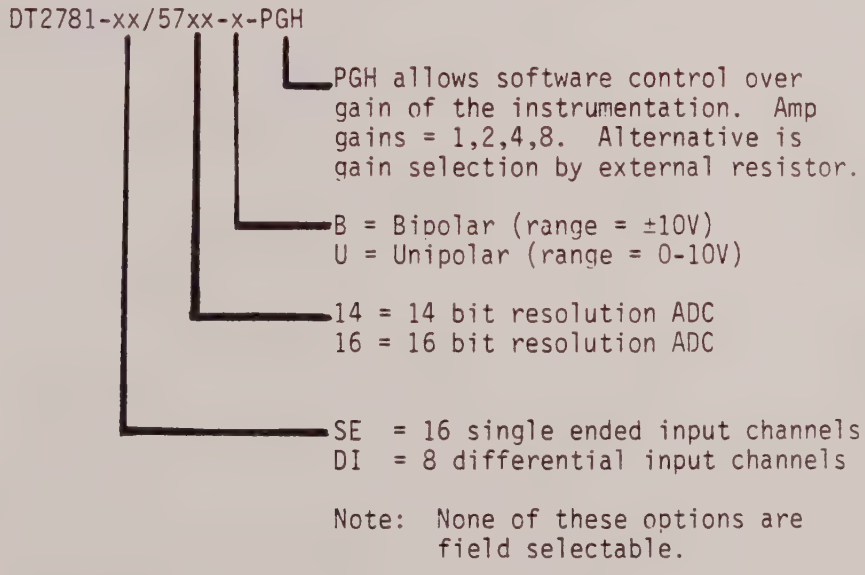
1.0 Product Description

DTI has designed a series of DEC dual height LSI Q-Bus compatible analog I/O boards. All models come standard with two independent D/A converters as well as a 16 single ended (8 differential) input A/D converter system. For clarity, the products have been broken up into two categories.

High Level Inputs

DT2781 - 12 bit resolution ADC with field selectable ranges of 0-10V (unipolar) or ±10V (bipolar). Has 16 single-ended or 8 differential input channels. SE/DI is field selectable, optional high level programmable gain option is also available, which provides gains of 1,2,4, & 8.

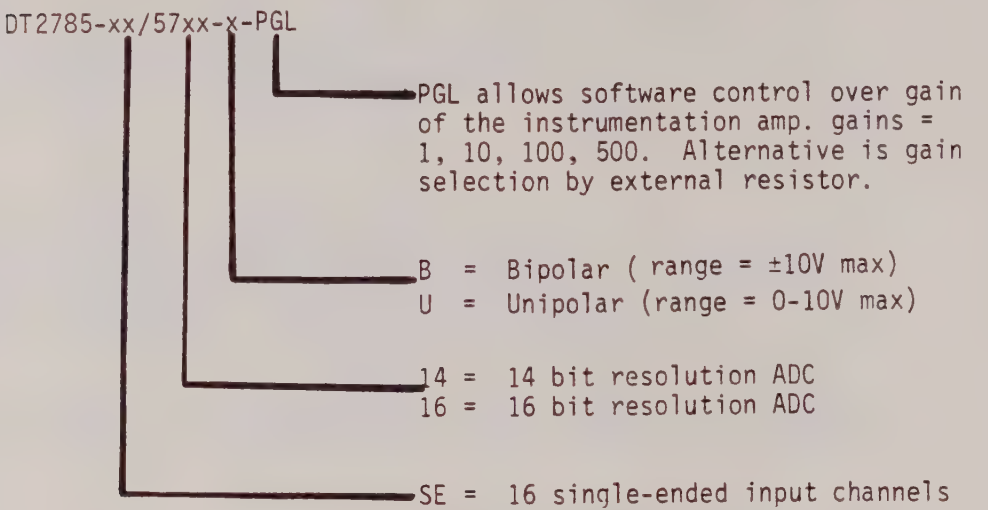
DT2782/15xx - Same as above except with higher resolution on ADC. Configuration is not field selectable. Can be ordered as follows:


DT2781-xx/57xx-x-PGH
PGH allows software control over gain of the instrumentation. Amp gains = 1,2,4,8. Alternative is gain selection by external resistor.
B = Bipolar (range = ±10V)
U = Unipolar (range = 0-10V)
14 = 14 bit resolution ADC
16 = 16 bit resolution ADC
SE = 16 single ended input channels
DI = 8 differential input channels
Note: None of these options are field selectable.

Wide Range Inputs

DT2785 - 12 bit resolution ADC with field selectable unipolar or bipolar operation. Ranges are resistor selectable from 0-10mV unipolar (±10mV bipolar) to 0-10V unipolar (±10V bipolar). Has 16 single-ended or 8 differential input channels. SE/DI is field selectable. An optional low level programmable gain option providing gains of 1, 10, 100, 500 is also available in place of resistor programmed range.

DT2785/57xx - Same as above except with higher resolution on ADC. Configuration is not field selectable. Can be ordered as follows:


DT2785-xx/57xx-x-PGL
PGL allows software control over gain of the instrumentation amp. gains = 1, 10, 100, 500. Alternative is gain selection by external resistor.
B = Bipolar (range = ±10V max)
U = Unipolar (range = 0-10V max)
14 = 14 bit resolution ADC
16 = 16 bit resolution ADC
SE = 16 single-ended input channels
DI = 8 differential input channels

Note: None of these options are field selectable

CHAPTER 2

2.0 DT2781 High Level Input System Specifications

2.1 Analog Inputs

The DT2781 (12-bit version) utilizes the DT5712 data acquisition module. This module will accept up to 16 single-ended or 8 differential input channels. SE/DI selection is accomplished by wire wrap jumpers. This board has no expansion capability.

2.2 Number of Analog Inputs

The DT2781 will accept up to 16 single-ended or 8 differential input channels.

2.2.1 Selection of SE/DI

The configuration is field selectable simply by altering wire wrap jumpers.

2.3 Input Range

0-10V F.S. straight binary (unipolar)
±10V F.S. 2's complement offset (bipolar)

2.3.1 Input Protection

Inputs are current limited and protected to an ± 35V overvoltage condition without damage.

2.3.2 Input Impedance

100 Megohm, 10pf - "off" channels
100 Megohm, 100pf - "on" channels

2.3.4 Input Bias Current

±0nA @ 25°C

2.3.5 Maximum Input Signal

11.0 Volts (signal + common mode voltage)

2.3.6 Common Mode Rejection Ratio

80 dB at full scale

2.4 A/D Specifications

2.4.1 Resolution

12 bits - unipolar
11 bits + sign bit - bipolar

2.4.2 Linearity

±½LSB

2.4.3 Inherrent Quantisizing Error

±½LSB

2.4.4 Stability

±30ppm/°C FSR

2.4.5 Sample and Hold Aperture Uncertainty

<10nSEC.

2.5 System Specifications

2.5.1 System Accuracy

±.03% (Bipolar)

2.5.2 Throughput Rate

40KHz

2.5.3 Input Noise

2uV RMS

CHAPTER 3

3.0 DT2781/57xx High Resolution, High Level Input System Specifications

3.1 Analog Inputs

The DT2781/57xx uses the DT5714/DT5716 modules for higher ADC resolution. This option will also accept 16 single-ended or 8 differential input channels. The SE/DI configuration is not jumper selectable and there is no expansion capability.

3.2 Input Specifications

3.2.1 Input Range

0-10V F.S. straight binary (unipolar)
±10V F.S. 2's complement offset (bipolar)

The input range can be changed under software control by the PGH option or hardware control via an external resistor. See table 1 and product description. The gains possible are 1,2,4,8.

3.2.2 Input Protection

Inputs are current limited and protected to ± 16V.

3.2.3 Input Impedance

100 Megohm, 10pf "off" channel
100 Megohm, 100pf "on" channel

3.2.4 Input Bias Current

15nA @ 25°C

3.2.5 Maximum Input Signal

10.5V (signal + common mode voltage)

3.2.6 Common Mode Rejection Ratio

80 dB at F.S.

3.3 5714 A/D Specifications

3.3.1 Resolution

14 bits

3.3.2 Linearity

±½LSB

3.3.3 Inherent Quantisizing Error

±½LSB

3.3.4 Offset Error

Adjustable to zero

3.3.5 Gain Error

Adjustable to zero

3.3.6 Stability

± 10ppm/°C FSR

3.3.7 Accuracy

±.01%

3.3.8 Throughput

10KHz

3.3.9 Input Noise

1uV RMS

3.4 5716 A/D Specifications

3.4.1 Resolution

16 bits

3.4.2 Linearity

- 1 LSB

3.4.3 Inherent Quantisizing Error

± 1 LSB

3.4.4 Stability

±10ppm/°C FSR

3.4.5 Accuracy

±.0075% at gain = 1. If PGH option is used, see table 1.

3.4.6 Throughput

2.4KHz at gain = 1. If PGH option is used, see table 1.

3.3.7 Input Noise

1uV RMS

CHAPTER 4

4.0 2785 Wide Range Input Specifications

4.1 Analog Inputs

The DT2785 utilizes the 5712 wide range data acquisition module. This module will accept up to 16 single-ended or 8 differential input channels. SE/DI selection is accomplished by wire wrap jumpers. There is no expansion capability.

4.2 Number of Analog Inputs

The DT2785 will accept upto 16 single-ended or 8 differential input channels.

4.2.1 Selection of SE/DI

The configuration is field selectable simply by altering wire wrap jumpers.

4.3 Input Range

The input range is variable by changing Rg and Ct (see Figure 8 for location). Full scale extends from 10mV to 10V in either the unipolar or bipolar mode. See table 1 for details.

4.3.1 Input Protection

Inputs are current limited and protected to ± 30V overvoltage without damage.

4.3.2 Input Impedance

100 Megohm, 10pF - "OFF" channel
100 Megohm, 100pF - "ON" channel

4.3.3 Input Bias Current

20 nA @ 25°C

4.3.4 Maximum Input Signal

± 11.0V (signal + common mode

4.3.5 Common Mode Rejection Ratio

80dB at full scale

4.4 A/D Specifications

4.4.1 Resolution

12 bits - unipolar
11 bits + sign bit - bipolar

4.4.2 Linearity

$\pm\frac{1}{2}$LSB

4.4.3 Inherent Quantisizing Error

$\pm\frac{1}{2}$LSB

4.4.4 Stability

± 30 ppm/°C FSR

4.4.5 Sample and Hold Aperture Uncertainty

<10nSEC

4.5 System Specification

4.5.1 System Accuracy and Throughput

System accuracy and throughput depend upon the range setting of the A/D system. Table 1 shows how these quantities inter-relate.

4.5.2 Input Noise

2uV RMS

INPUT RANGE *		GAIN	** Rext (in Ohms)	Cext	AMPLIFIER SETTLING TIME (uS)	SYSTEM ACCURACY	*** THROUGHPUT
Unipolar	Bipolar						
0 to +10mV	±10mV	1000	20.02	0.015uf	250	±0.1%	3.8KHz
0 to +25mV	±25mV	400	50.13	6800pf	120	±0.08%	7.5KHz
0 to +50mV	±50mV	200	100.5	3300pf	70	±0.07%	12KHz
0 to 100mV	±100mV	100	202.0	1500pf	40	±.05%	20KHz
0 to +1V	±1V	10	2222	NONE	15	±.03%	40KHz
0 to +2.5V	±2.5V	4	6667	NONE	15	±.03%	40KHz
0 to +5V	±5V	2	20.0K	NONE	15	±.03%	40KHz
0 to +10V	±10V	1	NONE	NONE	15	±.03%	40KHz

TABLE 1.0

INPUT RANGE PARAMETERS FOR 12-BIT A/D MODEL

INPUT RANGE				Cext (in uF)		AMPLIFIER SETTLING TIME (in Millisec)		SYSTEM ACCURACY		THROUGHPUT RATE (in Hz)	
Unipolar	Bipolar	GAIN	Rext (in Ohms)	DT5716	DT5714	DT5716	DT5714	DT5716	DT5714	DT5716	DT5714
0 to +5mV	±5mV	2000	50.02	0.470	0.100	24.0	6.0	±.13%	±.14%	40	166
0 to +10mV	±10mV	1000	100.10*	0.220	0.056	12.0	3.0	±.06%	±.08%	80	333
0 to +25mV	±25mV	400	250.62*	0.082	0.022	4.8	1.2	±.035%	±.040%	200	833
0 to +50mV	±50mV	200	502.51*	0.039	0.010	2.4	.6	±.020%	±.022%	400	1600
0 to 100mV	±100mV	100	1,010.1*	.022	0.0047	1.2	.3	±.010%	±.020%	800	3300
0 to +1V	±1V	10	11,111*	None	None	.3	.07	±.010%	±.015%	2500	10,000
0 to +2.5V	±2.5V	4	33,333*	None	None	.3	.07	±.010%	±.012%	2500	10,000
0 to +5V	±5V	2	100,000*	None	None	.3	.07	±.009%	±.01%	2500	10,000
0 to +10V	±10V	1	NONE	None	None	.3	.07	±.0075%	±.01%	2500	10,000

* These resistors are offered as a Precision Resistor Gain Selection Kit, Model number DT13-10501-4, for high accuracy gain setting

$$\text{Throughput Time} = \frac{1}{\text{Amplifier Settling Time} + \text{A/D Conversion Time}} \qquad R_{EXT} = \frac{100{,}000}{(G-1)}$$

TABLE 2.0

INPUT RANGE PARAMETERS FOR 14 & 16 BIT A/D MODELS

CHAPTER 5

5.0 DT2785/57xx High Resolution, High Level Input System Specifications

5.1 Analog Inputs

The DT2785/57xx uses the 57xx wide range modules for higher resolution as well as variable gain setting. This option will also accept 16 single-ended or 8 differential input channels. Configuration is not jumper selectable. There is no expansion capability.

5.2.1 Input Range

Input range is variable by either changing Ct/Rg or by using the PGL option. PGL gives gains of 1,10,100, and 500. See table 2 for details.

5.2.2 Input Protection

Inputs are current limited and protected to ±16V overvoltage without damage.

5.2.3 Input Impedance

100 Megohm, 10pF "off channel"
100 Megohm, 100pF "On channel"

5.2.4 Input Bias Current

15mA @ 25°C

5.2.5 Maximum Input Signal

±10.5Vs (signal + commode mode voltage)

5.2.6 Commode Mode Rejection

80 dB

5.3 5714 A/D Specifications

5.3.1 Resolution

14 bits

5.3.2 Linearity

±1 LSB

5.3.3 Inherent Quantisizing Error

±1 LSB

5.3.4 Offset Error

Adjustable to zero

5.3.5 Gain Error

Adjustable to zero

5.3.6 Stability

±10ppm/°C FSR

5.3.7 System Accuracy and Throughput

System accuracy and throughput depend upon the range setting of the A/D system. Table 2 shows how these quatities interrelate.

5.3.8 Input Noise

1uV RMS

5.4 5716 A/D Specifications

5.4.1 Resolution

16 bits

5.4.2 Linearity

±1LSB

5.4.3 Inherent Quantisizing Error

-1LSB

5.4.4 Stability

±10ppm/°C FSR

5.4.5 Accuracy and Throughput

System accuracy and throughput depend upon the range setting of the A/D system. Table 2 shows how these quantities interrelate.

5.4.6 Input Noise

1uV RMS

CHAPTER 6

6.0	External Trigger Specifications for All Models (EXT Trig L, Pin 19-J1)	
6.0.1	Signal Compatibility	TTL
6.0.2	Origin	User device (i.e. DT2769 Real Time Clock, or Signal Generator.)
6.03	Usage	To initiate A/D Conversion (Note: trigger occurs on high to low edge only.)
6.0.4	Loading	1 TTL Load.
6.1	D/A Specifications (both Channels) on all Models	
6.1.1	Resolution	12 bits
6.1.2	Non-Linearity	.02%
6.1.3	Differential Linearity	+/- ½ LSB
6.1.4	Gain Error	adjustable to zero
6.1.5	Zero Error	adjustable to zero
6.1.6	Offset drift unipolar	+/- 3ppm/ C
6.1.7	Offset drift bipolar	+/- 30ppm/ C
6.1.8	Gain drift	+/- 30ppm/ C
6.1.9	Settling Time	
6.1.10	to 0.01% FSR	35uS (10 Volt step)
6.1.11	Settling Time	
6.1.12	to 0.01% FSR	10uS (0.1 volt step)
6.1.13	Slew Rate	0.33 V/USEC
6.1.14	Range	0-10V, ±10V, ±5V (jumper selectable)
6.1.15	Current Output Impedance (DC)	±5mA Max. 0.1 ohms.
6.1.16	Noise	0.1% FSR
6.1.17	Capacitive Load Capability	0.5 MFD
6.1.18	Protection	Short Circuit Protected to Common

6.2 Physical Specifications

All models are contained on a standard DEC dual height card with LSI-11 compatability.

6.3 Power Requirements

All models - +5V @ 1.5A 5%

6.4 Q-Bus Loading

Each card represents 1 Q-Bus load.

CHAPTER 7

7.0 Programming Specifications for All Models

Data Translation interfaces are designed to meet the requirements of standard DEC interfaces. As such they are structured around a Control and Status register for complete software control of the interface.

7.1 DT2781/DT2785

7.1.1 Modes of Operation

This series can operate in a number of operating modes, as follows:

Program I/O - In this mode standard LSI-11 instructions can access and control the A/D components on the interface. A start A/D conversion can be accomplished by two ways:

1. Set A/D Start Bit (Bit Ø) ADCSR

2. External Triggers or Real Time Clock input.

Interrupt - In many real time applications the program does not want to dedicate itself to taking analog measurements. In this case the interface can be enabled to produce a program interrupt on the condition A/D Done. An interrupt may also be produced on the Error bit (Bit 15 ADCSR).

7.1.2 Device Address

The DT2781/DT2785 device address is selectable via wire wrap jumpers. Device address may be assigned between 170000_8 and 177770_8. The order of address is as follows, once a base address has been set in the jumpers:

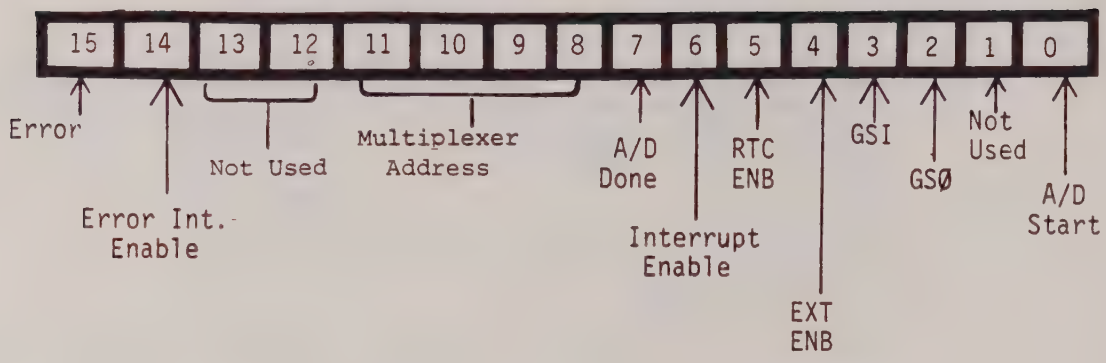
A/D Control and Status Register (ADCSR) - Base (R/W)
A/D Data Buffer Register (ADDBR) - Base + 2 (Read only)
DAC A Register - Base + 4 (Write Only)
DAC B Register - Base + 6 (Write Only)

7.1.3 Interrupt Vector Address

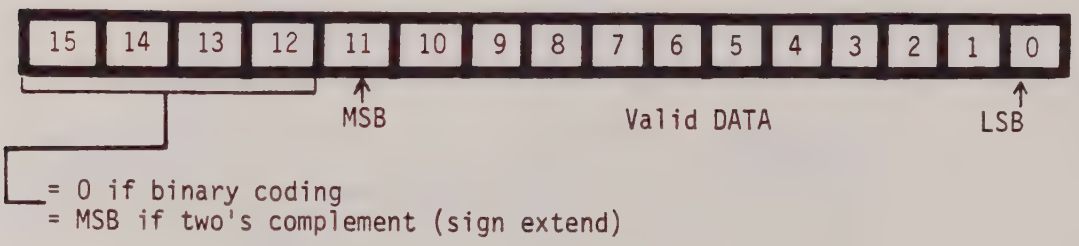
The vector address is set via wire wrap jumpers, they are selectable in increments of 10_8. There are two interrupts A/D DONE, and ERROR. (See 7.1.4 CSR descriptions).

A/D DONE = BASE VECTOR
ERROR = BASE VECTOR + 4.

7.1.4 Control and Status Register



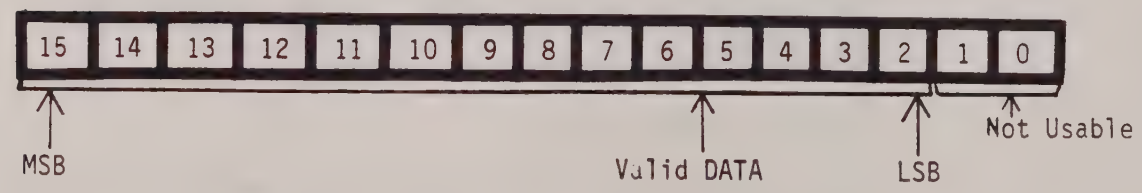
7.1.5 DT2781/2785 A/D Data Buffer Register (ADDBR) (Read Only)



The user has the option of using bits 12-15 in either sign extend mode or hard wiring to logic Ø-1

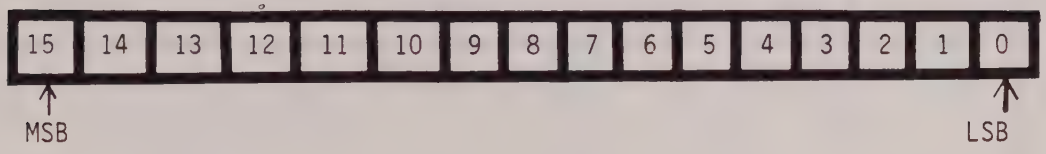
7.1.6 DT2781/5714 A/D Buffer Register (Read only)

For 14 bit resolution, the two least significant digits are ignored.



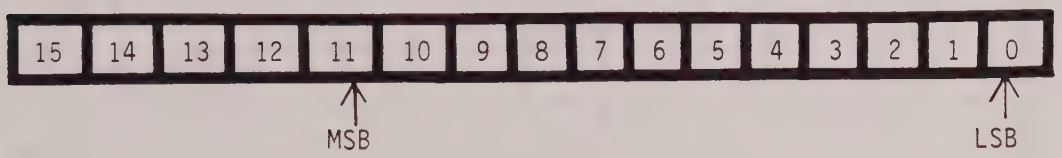
7.1.7 DT2781/5716 A/D Buffer Register (Read Only)

The format for 16 bit resolution is as follows:



7.1.8 D/A Data Registers (Write Only)

The 12 bit D/A Registers are loaded in the following format:



The conversion is started immediately upon loading.

CSR BIT DESCRIPTIONS: Note:

<table>
<tr><th>BIT #</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>15</td><td>ERROR</td><td>READ/WRITE - Indicates an error set by one of the following conditions.

1. Attempting an external start or clock start during MUX settling.

2. Attempting a start while conversion in process.

3. Attempting any start while the A/D Done bit is set.

Cleared by Processor and Init</td></tr>
<tr><td>14</td><td>ERROR INT. ENABLE</td><td>READ/WRITE - When set enables an Interrupt on Error Bit. Cleared by INIT.</td></tr>
<tr><td>13-8</td><td>MULTIPLEXER ADDRESS</td><td>READ/WRITE - Six MUX channel address bits. Only 4 Bits are used.</td></tr>
<tr><td>7</td><td>A/D DONE</td><td>READ ONLY - Set by end of conversion reset by read A/D data. Cleared by INIT.</td></tr>
<tr><td>6</td><td>DONE INT. ENABLE</td><td>READ/WRITE - When set will enable interrupts from A/D done. Cleared by INIT.</td></tr>
<tr><td>5</td><td>RTC ENB</td><td>READ/WRITE - Real time clock enable when set this bit allows start conversion from the real time clock.</td></tr>
<tr><td>4</td><td>EXT TRIG ENB</td><td>READ/WRITE - When set this bit allows start conversion from an external trigger source.</td></tr>
<tr><td>3-2</td><td>GAIN SELECT</td><td>READ/WRITE - These bits provide the gain select information for PGX option
<table>
<tr><th>BIT 3 (GS1)</th><th>2 (GSØ)</th><th>PGH</th><th>PGL</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>2</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>4</td><td>100</td></tr>
<tr><td>1</td><td>1</td><td>8</td><td>500</td></tr>
</table></td></tr>
<tr><td>Ø</td><td>A/D START</td><td>WRITE ONLY - Initiates a conversion when set, cleared by internal logic after start conversion, will always read back as a Ø.</td></tr>
</table>

CHAPTER 8

8.0 User Configuration

8.1 Base Address Selection For All Models

The Base Address which is the I/O address assigned to the Control-Status Register (CSR) is user selectable by means of wire wrap jumpers located near the bus interface logic as shown in Figure 8.3. The A/D Data Buffer Register address is then two locations greater than the CSR (Base) address. The DIP switches allow the user to set the base address anywhere in the 170000_8 - 177774_8 address space in increments of 10_8. The recommended base address for the DT2781 series is 170400_8 and is the address set at the factory. Figure 8.1 shows how the wire wrap jumpers must be set to generate this base address.

1		7			0			4			0			0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0

Figure 8.1

Jumper Configurations for Base Address of 170400_8

As shown in Figure 8.1, a wire wrap jumper in place represents a "1" in the corresponding bit location and no wire wrap jumper represents a "0" in the corresponding bit location.

8.2 Vector Address Selection for All Models

The DT2781 series systems are capable of generating two distinct interrupt vectors to the LSI-11 processor. These interrupts can occur when:

1. A/D Done is set
2. Error is set

Each of these two events can generate a unique interrupt to the processor with the internal priority being arranged such that the A/D Done interrupt has the higher priority of the two if both occur simultaneously and are both enabled. The interrupt vector address of the A/D Done interrupt can be assigned any address in the 000_8 - 770_8 vector address space in 10_8 increments. The interrupt vector of the Error Interrupt is then always 4_8 locations higher than the A/D Done interrupt vector address. The recommended interrupt vector address for the DT2781

series is 400_8 and is set to that value at the factory. Figure 8.2 shows how the wire wrap jumpers must be set to generate this address.

0		0		0		4		0		0	
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

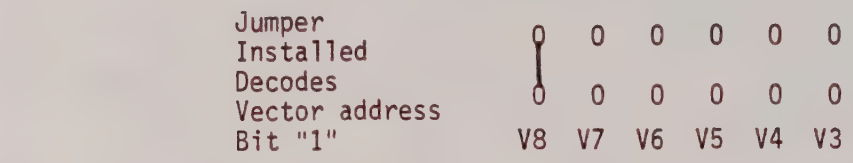


Figure 8.2

Jumper Configuration for Vector Address of 400

8.3 Analog Configuration for DT2781/DT2785

The input range, polarity, and data coding for 12-bit models are user selectable. High resolution models (14,16-bits) are not user configurable and must be ordered from the factory as required.

All user configuration is accomplished by the insertion or removal of a wire wrap jumper between a pair of posts.

The location of most of the posts have been lettered right on the P.C. board, however, for ease of location, figure 8.3a and figure 8.3b also show the locations of all the jumpers.

Please note that there are two types of jumpers on the board. Some of the jumpers are point-to-point in which case each wire wrap post has a unique number and jumpering is done from a certain wire wrap post to another numbered wire wrap post. The other jumpers are a labelled pair of wire wrap posts. With this type of designation a jumper is installed across a pair of wire wrap posts as identified in the configuration chart.

8.3.1 Ranges

The DT2781/85 have the following ranges:

DT2781 (High Level)	0-10V Unipolar or (0-5, 2.5 0-1.25 with PGH) ±10V Bipolar or (±5, ±2.5, ±1.25 with PGH)
DT2785 (Wide Range)	From 0-10mV F.S. to 0-10V F.S. From ±10mV F.S. to ±10V F.S. Resistor selectable, Unipolar or Bipolar (If PGL is selected then the resistor programmable option is deleted.)

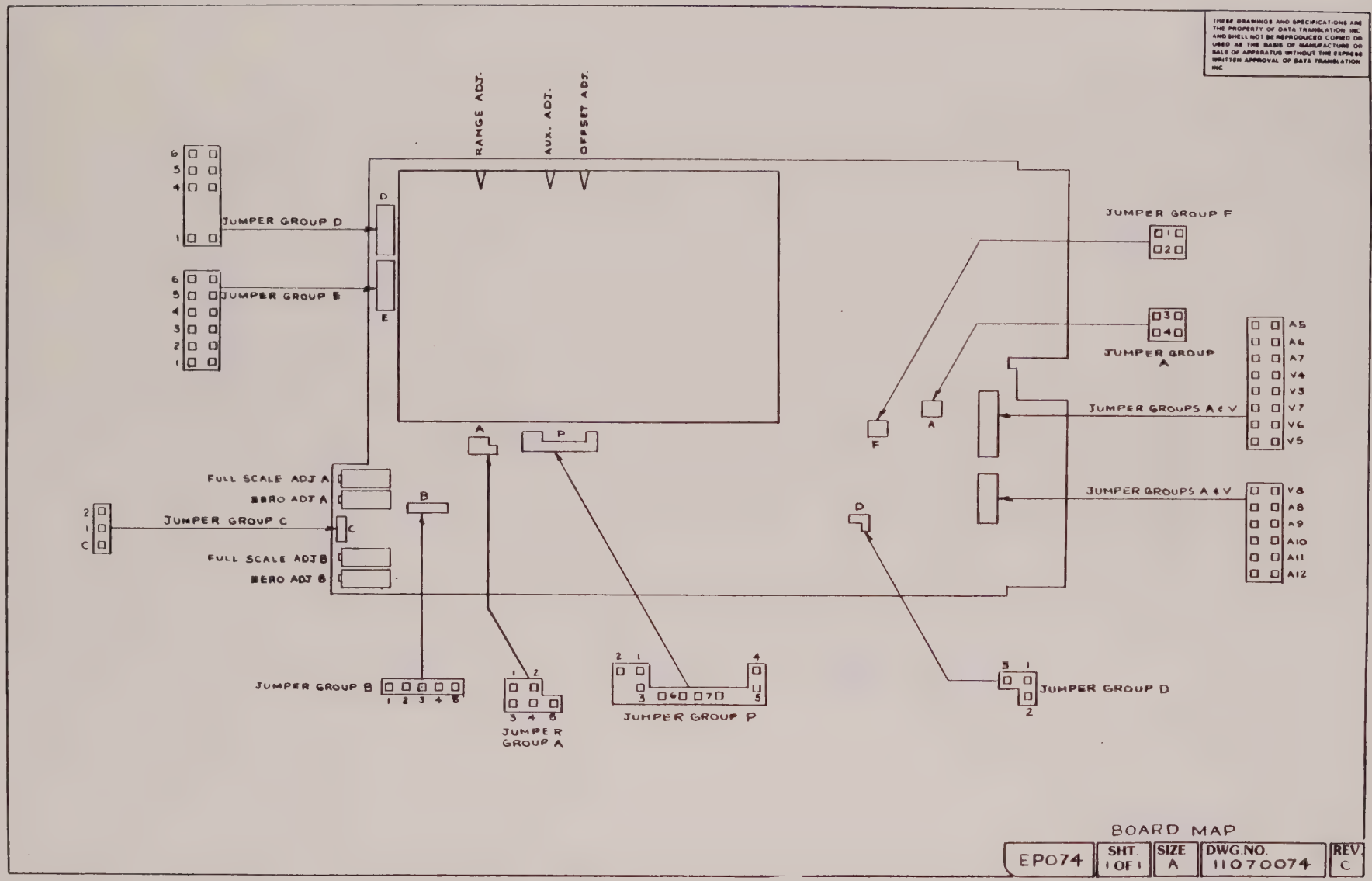
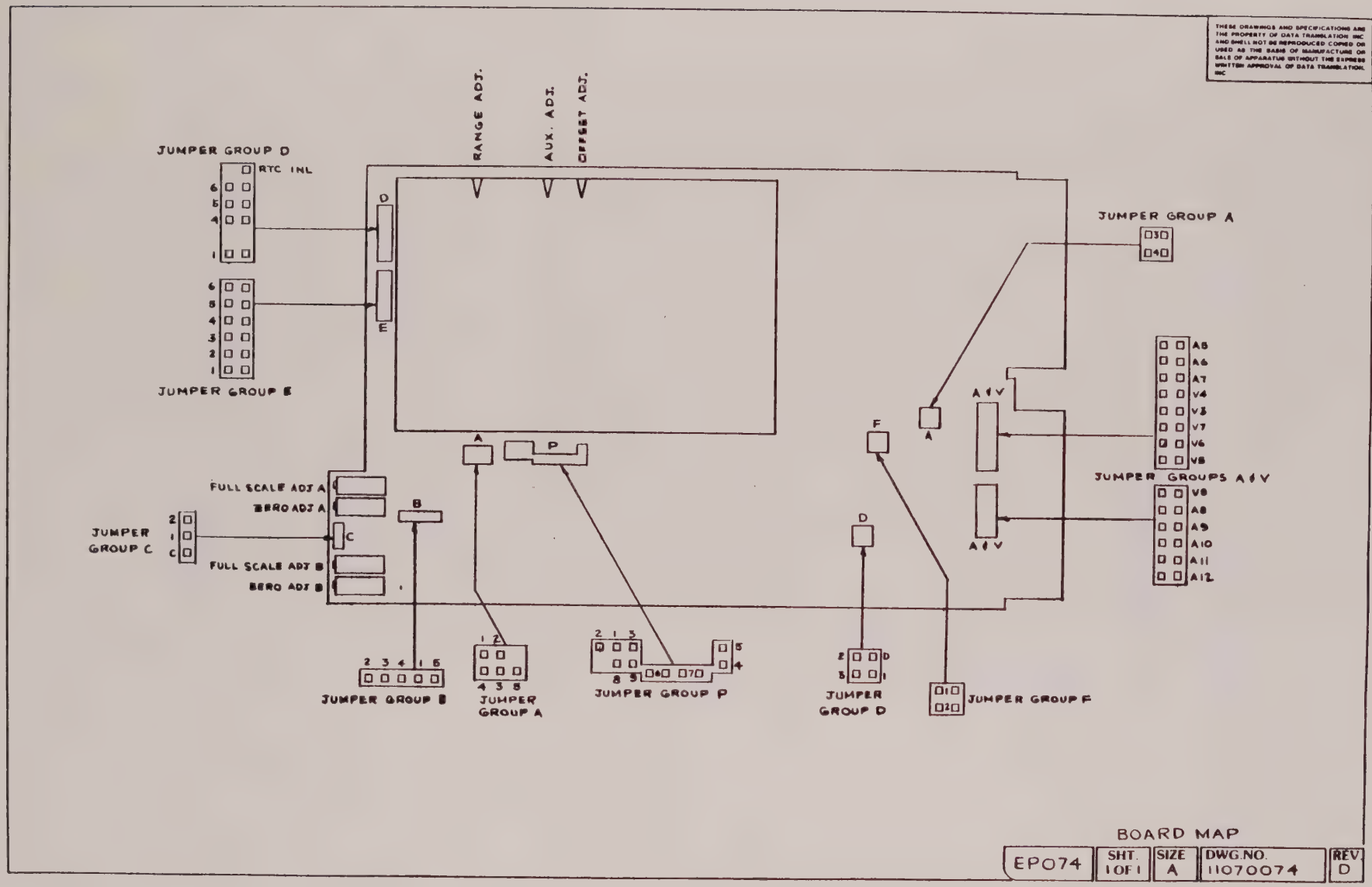


Figure 8.3a

Location of jumpers
for REV A - REV C Boards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RANGE ADJ.
AUX. ADJ.
OFFSET ADJ.
JUMPER GROUP D
RTC INL
JUMPER GROUP E
JUMPER GROUP A
JUMPER GROUPS A & V
FULL SCALE ADJ A
ZERO ADJ A
FULL SCALE ADJ B
ZERO ADJ B
JUMPER GROUP C
JUMPER GROUP B
JUMPER GROUP A
JUMPER GROUP P
JUMPER GROUP D
JUMPER GROUP F
BOARD MAP
EP074
SHT. 1 OF 1
SIZE A
DWG.NO. 11070074
REV D

Figure 8.3b

Location of jumpers
for REV H and later boards

8.3.2 DT2781/DT2785 Analog Input Configuration

Models DT2781/DT2785 can be user configured for SE or DI operation in the field. To change the DT2781/2785 from 16 SE to 8 DI or from 8 DI to 16 SE the following jumpers are required.

INPUT TYPE	JUMPERS
SE (16 Channels)	P1 to P2 P8 to P9
DI (8 Channels)	P2 to P3 and P4 to P5

(See Note below)

Note: 1) Factory default is DI.
2) P8 and P9 jumpers are only required for REV D and later boards. REV A - C do not have the P8 and P9 jumper posts.

8.3.3 DT2781/DT2785 Range Selection (with the programmable gain option)

The DT2781/DT2785 can be configured for any full scale range in the 10mV-10V range or ±10mV - ±10V by means of a single gain resistor. The gain resistor is used to program the gain of the instrumentation amplifier from 1 to 1000. Then as the A/D has a fullscale range of 10V or ±10V, the gain of the instrumentation amplifier will determine the full scale input signal required to produce a 10V or ±10V output. At a gain of 1000, the input signal voltage will be 10mV full scale. For a gain of 1, no resistor is required as the instrumentation amplifier is defaulted to this value internally. The gain of the instrumentation amplifier in terms of the gain selection resistor Rg is:

$$G = 1 + \frac{2 \times 10^4}{Rg}$$

or

$$Rg = \frac{2 \times 10^4}{G-1}$$

As the gain of the instrumentation amplifier is increased, the time allowed for the amplifier to settle must also be increased. This is accomplished by the addition of a single timing capacitor Ct. The location of the Rg resistor and Ct capacitor is printed on the interface board. The table below shows the resistors and capacitors required for some standard ranges.

CHART OF INPUT RANGE PARAMETERS

Input Range	Gain	RG (ohms)	Ct	System Accuracy	Amplifier Settling	Throughput
10mV, ±10mv	1000	20.02	0.015uf	±0.1%	250uS	3.8KHz
15mV, ±25mV	400	50.13	6800pf	±0.08%	120uS	7.5KHz
50mV, ±50mV	200	100.5	3300pf	±.07%	70uS	12.0KHz
100mV, ±100mV	100	202.0	1500pf	±.05%	40uS	20.0 KHz
1.0V, ±1.0V	10	2222	None	±.03%	15uS	40KHz
2.5V, ±2.5V	4	6667	None	±.03%	15uS	40KHz
5.0V, ±5.0V	2	20.0K	None	±0.03%	15uS	40KHz
10.0V, ±10.0V	1	None	None	±0.03%	15uS	40KHz

Note: Throughput = $\frac{1}{\text{Amp Settling} + 20\text{uS}}$

8.3.4 DT2781/DT2785 Input Polarity Selection

By using an appropriate Rg and Ct the user can configure the range of operations as required, the polarity of the input and data coding is then selected via jumpers as outlined below:
Note: These jumpers are configured as pairs thus installing jumper 1D means put a wire across the pair of posts labelled 1D.

POLARITY	JUMPERS		
	TWO's COMPLEMENT DATA	OFFSET BINARY DATA	BINARY DATA
Unipolar	Not applicable	Not applicable	1D, 6D, 6E
Bipolar	4D, 5D, 5E	4D, 6D, 6E	Not applicable

8.4 Analog Configuration for DT2781/57xx and DT2785/57xx

8.4.1 Ranges

Both models have the capability of user selectable gain of the input amplifier. This can be done using the PGX option or by adding an external resistor. See table 8.4 and sections 8.4.2, 8.4.3.

8.4.2. PG Option

The PGX option can be ordered with high resolution A/D modules. It allows software control over the F.S. input range. Note that a timing cap of .022uF (14 bit) or .062uF (16 bit) must be installed for proper PGH operation. Also, install jumpers P6 and P7.

PGH (2781/57xx)

GAIN	RANGE
1	0-10V, ±10V
2	0-5V, ±5V
4	0-2.5V, ±2.5V
8	0-1.25V, ±1.25V

PGL (2785/57xx only)

GAIN	RANGE
1	1-10V, ±10V
10	0-1V, ±1V
100	0-100mV, ±100mV
500	0-20mV, ±20mV

8.4.3 Gain Selection with PGX

If no PGX option is present, then gain can be selected by an external resistor (Rg) and external capacitor (Ct). The gain equation for the instrumentation amp. is

$$G = \frac{1 + 100{,}000}{Rg} \quad \text{or} \quad Rg = \frac{100{,}000}{G-1}$$

See chart of Input Parameters (table 8.4)

8.4.4 Selection of SE/DI and U/B

None of the higher resolution models are field selectable in these parameters. They must be factory ordered. (See product description.)

8.4.5 Data Notation for 14 Bit Resolution

Parallel digital outputs are provided in binary code. A unipolar input (0 to F.S.) should be jumpered to produce a straight binary output. A bipolar input (±F.S.) can be jumpered to produce offset binary coding or 2's complement coding. The two least significant bits are ignored.

CODE	RANGE	16 BIT BINARY CODE
Binary	+F.S.	177774 - 177777
	0	000000 - 000003
Offset	+F.S.	177774 - 177777
	0	100000 - 100003
	-F.S.	000000 - 000003
2's Complement	+F.S.	077774 - 077777
	0	000000 - 000003
	F.S.	100000 - 100003

8.4.6 Data Notation for 16 Bits

Parallel digital outputs are provided in binary code. A unipolar input (0 to F.S.) should be jumpered to produce a straight binary output. A Bipolar input (±F.S.) can be jumpered to produce offset binary coding or 2's complement coding.

CODE	RANGE	16 BIT BINARY CODE
Binary	+F.S.	177777
	0	000000
Offset Binary	+F.S.	177777
	0	100000
	-F.S.	000000
2's Complement	+F.S.	077777
	0	000000
	-F.S.	100000

8.5 External Trigger Configuration[1]

The DT2781 series allows the user to synchronize A/D conversion from two external sources. Each of the two sources may be enabled or disabled individually by software by setting or clearing certain bits of the control and status register. The source designated as RTCINL is applied to the board via user connector J1 pin 21. The source designated as EXT TRIG. may be selected by the user to the signal applied at user connector J1 pin 19 or the BUS EVENT line (BEVENT L) which is a 50/60 cycle signal appearing on the computer bus. To select the source for the EXT TRIG. signal jumper pairs F1 and F2 are used as outlined below.

EXT TRIG. source comes from J1 pin 19 - Install F2.

EXT TRIG. source comes from BUS EVENT line - Install F1.[2]

NOTE: Only one of the F jumpers should be installed at a time.

8.6 D/A Configuration (All Models)

The output range, data, polarity and the format of the digital data presented to the DACs are user selectable as outlined in the tables below. Note that both DAC A and DAC B must operate with the same data coding and output polarity configuration. However, they need not both operate at the same range (i.e. DAC A may be strapped for ±10V full scale while DAC B may be strapped for ±5V full scale, and both must operate with the same data format, either two's complement or offset binary).

[1]Note on REV A - C boards the silk screen for F1 and F2 is reversed. Thus External Trigger from J1 - 19 is obtained by installing F1.

[2]Note that the BUS EVENT line triggering feature is not available on REV A - D interface boards.

Range & Polarity	Binary Data Format	Offset Binary Data Format	Two's Complement Data Format
±10V	Not applicable (N.A.)	3A to 5A H1 to H3	3A to 5A H to H2
±5V	N.A.	1A to 2A, 3A to 5A, H1 to H3	1A to 2A, 3A to 5A, H to H2
0-10V	1A to 2A H1 to H3	N.A	N.A
0-6.667V	1A to 2A, 3A to 4A, H1 to H3	N.A	N.A

JUMPER TABLE DAC A

Range & Polarity	Binary Data Format	Offset Binary Data Format	Two's Complement Data Format
±10V	N.A.	1B to 5B H1 to H3	1B to 5B H to H2
±5V	N.A.	2B to 3B, 1B to 5B, H1 to H3	2B to 3B, 1B to 5B H to H2
0-10V	2B to 3B H1 to H3	N.A.	N.A.
0-6.667V	2B to 3B, 1B to 4B, H1 to H3	N.A.	N.A.

JUMPER TABLE DAC B

NOTE:

Jumpers H, H1, H2, and H3 are labelled D, D1, D2, and D3 on some boards. In Figures 8.3a and 8.3b, Jumper Group H is labelled as Jumper Group D. Group H is located immediately below Jumper Group F in these figures.

9.0

Table 9.1 shows the various models and the connection schemes available.

MODEL	SE/DI JUMPER SELECTABLE	NUMBER OF INPUTS
DT2781	Yes	16SE/8DI
DT2781/57xx	No	16SE/8DI
DT2785	Yes	16SE/8DI
DT2785/57xx	No	16SE/8DI

Please note that there is no expansion capabilities on any of these models.

9.1 Single-Ended Inputs - 16 Channels

Single-ended analog inputs - Single-ended connections are those which have a common side that is referenced back to analog common of the system. The advantage of this scheme is that the user gets twice the number of channels in the same space. The major disadvantage is that the user gives up any common mode rejection he might obtain from a differential system.

Recommendations:

High level inputs, greater than 1V.
Short lead lengths, less than 15 ft.

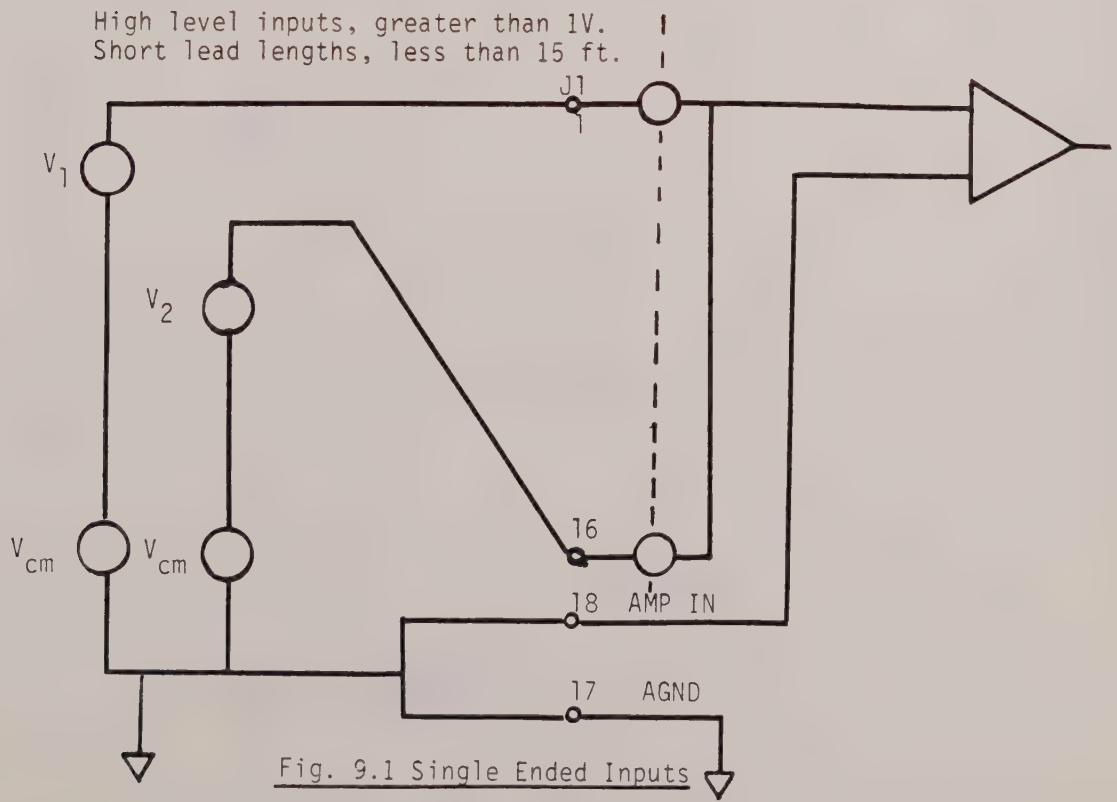


Fig. 9.1 Single Ended Inputs

Fig. 9.1 Single Ended Inputs (continued)

Where VCM = Common Mode Voltage

9.2 Pseudo - Differential Inputs - 16 Channels

Pseude - Differential mode can be utilized with a single ended system if the user has all input sensors referneced to a common ground point. In this manner the input instrumentation amplifier can reject common mode noise. This is possible since the AMP LO input is brought out to connector J1 for user connection. The following diagram illustrates -

Recommendation:

Input Ranges: 100mV to 10V
Lead Lengths - less than 25 ft.

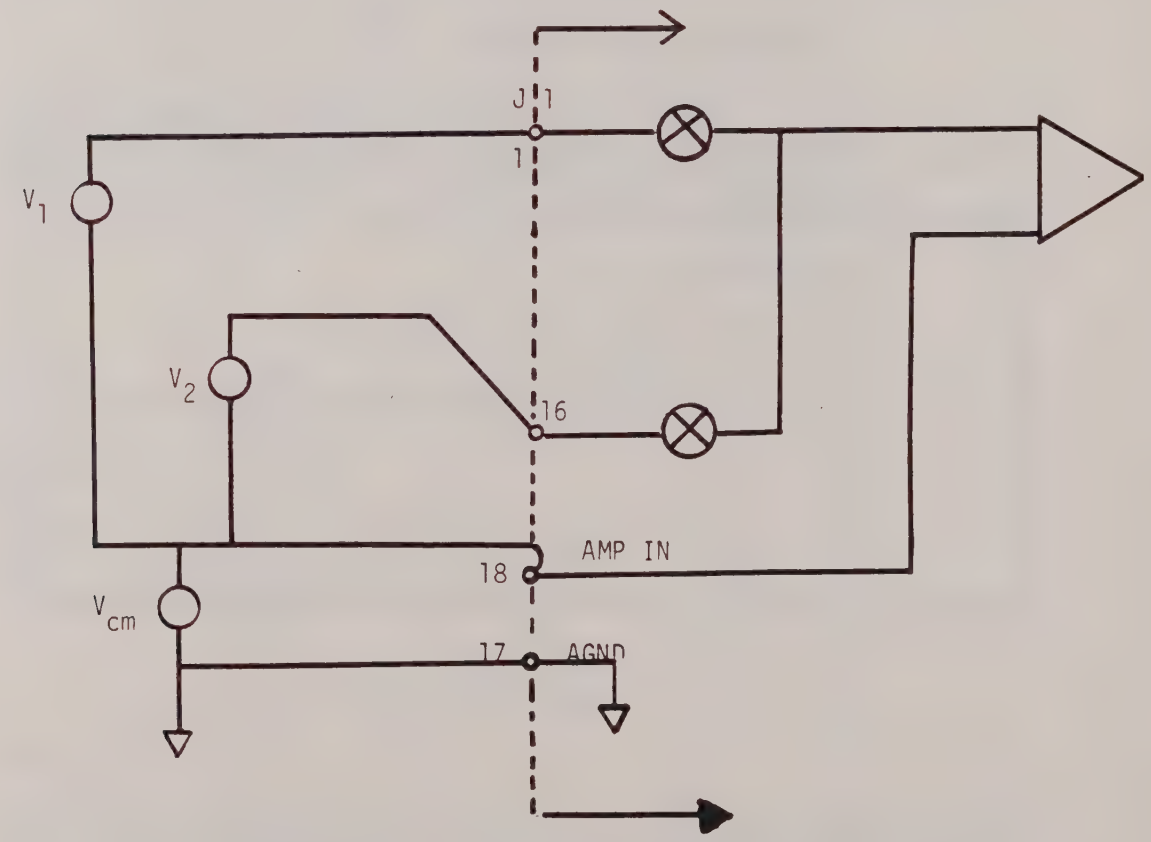


Fig. 9.2 PSEUDO-DIFFERENTIAL

9.3 Differential Inputs - 8 Channels

Differential Inputs - when the differential input scheme is utilized, there are two switches per channel, thus the number of channels are cut in half. The benefits are that common mode voltages, i.e. voltages appearing on both sides of the source simultaneously can be rejected by the differential input instrumentation amplifier. This CMR accounts for a much quieter system. The amount of CMRR depends on how well balanced the instrumentation amplifier is.

Recommendations:

Input Ranges:	10mV to 10V
Lead Lengths:	As required by user
Lead Type:	Twisted Pair (Low Level) Shielded Input line.

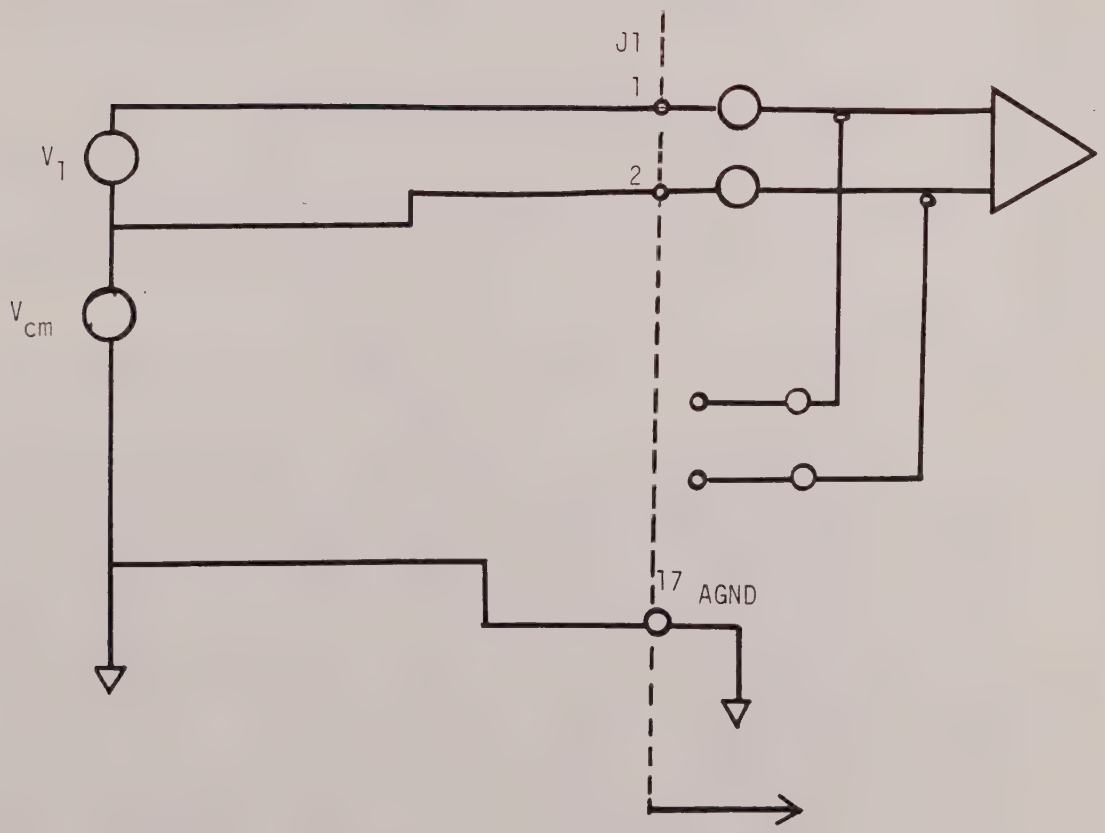


Fig. 9.3 DIFFERENTIAL INPUT CONNECTION

9.5 Avoiding Spurious Signals

In order to obtain the best performance from a system, certain guidelines in connecting analog signals to the system should be utilized. These guidelines and precautions will minimize the pickup of electrical noise by measuring circuits.

9.5.1 Twisted Pair Input Lines

The effects of magnetic coupling on the input signals may be reduced for differential input configuration by twisting the signal and return lines. This is effective since the inductive pickup voltages on the two lines tend to match, thus not having an effect on the measurement. This is not the case for a ground referenced single ended system.

9.5.2 Shielded Input Lines

The effects of electrostatic coupling may be reduced by shielding the input lines. This becomes important if the source has a high impedance. The shield should only be tied to ground at the instrument end. This will prevent ground loop currents.

9.5.3 Input Settling with High Source Impedance

Solid state multiplexers inject a small amount of charge into the input lines when channels are switched. This can cause a transient error due to the input source impedance time constants. All Data Translation systems allow for input settling upon new channel selection. The settling time varies for the different input systems available.

Normally, the control logic allows sufficient time for this charge to settle to less than ½LSB of error (nine time constants to .012 percent). However, more time may be needed when the multiplexer is switching an input channel with high source impedance, particularly when large amounts of shunt capacitance exists in the interconnecting cables. Source impedance/cable shunt capacitance products greater than 1 uSec (1K-1000PF) on 25KHz units should be avoided for less than 50PF/foot and 1K ohm source impedance.This translates into a maximum run of twenty feet on 25KHz models. Note also that settling errors can be minimized by increasing the internal time out with an external capacitor C_t (≈60PF per uSec).

9.6 Common Mode Rejection Ratio - (CMRR)

The CMRR of a system is defined as the ratio of output voltage from the instrumentation amplifier to the voltage which is common to both sides of the differential input amplifier. This ratio is given in units of decibels.

9.6
(Cont.)

For example, the specification for CMRR on Data Translation's wide range interface is 100db at 60HZ at a gain of 1000. Thus with a CMV of 10 volts, the V out of the amplifier at a gain of 1000 should be:

$$CMRR = 20\log_{10} \left(\frac{CMV}{VOUT/A}\right)$$

Where CMRR = common mode rejection in db
CMV = common mode voltage
VOUT = The change in the amplifier output voltage due to the CMV.
A = Amplifier gain

$$100 = 20\log_{10} \left(\frac{CMV}{VOUT/A}\right)$$

$$\text{Antilog } \left(\frac{100}{20}\right) = \frac{10^4}{VOUT/1000}$$

$$10^5 = \frac{10^4}{VOUT}$$

$$VOUT = 10^{-1} \text{ V.}$$

Thus with a CMV of 10 volts, the output of the instrumentation amplifier is 100 millivolts.

9.7 User Connections

User connections are made via a 26 pin 3M type connector. This connector contains all analog input lines, D/A output lines, and external trigger inputs.

J1 CONNECTOR

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	CHØ	2	CH8/RETØ
3	CH1	4	CH9/RET1
5	CH2	6	CH10/RET2
7	CH3	8	CH11/RET3
9	CH4	10	CH12/RET4
11	CH5	12	CH13/RET5
13	CH6	14	CH14/RET6
15	CH7	16	CH15/RET7
17	A GND	18	AMP IN
19	EXT TRIG L	20	D GND
21	RTCINL	22	D GND
23	DAC A RET	24	DAC A OUT
25	DAC B RET	26	DAC B OUT

NECTOR

RTCINL on Wire Post

9.8 External Trigger and RTC Inputs

This series of analog interfaces allow the user to externally trigger the conversion. Thus allowing sychronization of conversion to real word or a real time clock input. Data Translation can supply the user with a KVV11-A equivalent module, the DT2769 real time clock module. The two trigger inputs are only edge sensitive and initiate a conversion on the negative (high to low) transition of the input signal only.

CHAPTER 10

10.0 Calibration and Testing

10.1 Equipment and System Requirements

In order to assist the user in testing the operation of the DT2780 series interfaces, Data Translation has developed a comprehensive software diagnostic aid designated SP0031. This software is provided in either of the two media: Paper pape for minimum, paper tape based LSI-11 Systems, or Floppy Disks for more sophisticated RT-11 Systems. The system and test equipment requirements for this software are given below:

SP0031 - All models

SP0031 System Requirements
Paper Tape:

KD11-F (LSI-11) processor, ECO #10 or greater

or

KD11-HA (LSI-11/2) processor

Minimum of 4K words RAM
Serial Interface at Standard DEC console address
Paper tape reader
Data Translation DT2780 series interface.

Floppy Disk

KD11-F (LSI-11) processor, EC) #10 or greater

or

KD11-HA (LSI-11/2) processor

Minimum of 8K words RAM
System console terminal at standard DEC console address
DEC compatible dual floppy disc drive system
RT-11 operating system (Version 2 or Version 3)
Data Translation DT2780 series interface

Test Equipment Requirements

10MHz or greater bandwidth oscilloscope
Laboratory quality voltage standard

10.2 Loading SP0031 from Paper Tape

This software is supplied in PDP-11 absolute loader format. To load this release into memory the following steps must be taken:

1. Load the LSI-11 absolute loader (see DEC documentation for information on this.)

10.2
(Cont.)

2. Place the paper tape in the paper tape reader.

3. Start the absolute loader at location XXX500 where XXX is determined by the following table: (See 10-2)

System Memory Size	XXX
4K	017
8K	037
12K	057
16K	077
20K	017
24K	137
28K or greater	157

Following this procedure will cause SP0023 to be loaded into memory and executed.

10.2.1 Loading Floppy Disk

The SP0031 diskette contain an RT-11 memory image file called SP0031 SAV. This is a linked and executable version of SP0023. To load and execute SP0031, the user should boot up RT-11 in the usual way with the system disk in drive Ø. When RT-11 comes up the user should insert the SP0031 disk into drive 1 and type the following command string to the RT-11 monitor;

RUN DX1:SP0031 (Return)

This will cause SP0031 to be loaded and executed, at this time the SP0031 monitor will have control of the system and RT-11 will be prevented from interfacing.

10.3 Using SP0031

SP0031 is a stand-alone software diagnostic package that allows the user to test Data Translation's dual-height series of LSI-11 interface cards. The test program does not need RT-11 once it has been loaded and in fact it flushes RT-11 from the system after it has loaded. To allow the user to control the testing procedure a monitor has been included that interfaces to the user. When SP0031 is brought up this monitor is automatically entered. On start up the resident monitor prints out the directory of the various Data Translation interface boards that can be tested followed by the monitor prompt character ">" (a right angle-bracket). At this point the user should set the desired model number to be tested using the MODEL command.

10.3
(Cont.) for example:

Model (Space) DT2781 (Return)

would set up the program to test the DT2781 Analog Input Board. The monitor would then invoke all the necessary initialization routines to test this board and confirm the board model by printing out a confirmation message followed by the default base and vector addresses that will be used. These base and vector addresses have been preset at the factory and need not be changed. If for some reason, however, a change in the base or vector address is required, the user can modify locations 542 (base address) and 544 (Vector address) to the new address. In order to easily facilitate this change the SP0031 monitor also has some subset capabilities of ODT. In particular, the user can use the slash and back-slash characters to open and modify memory locations just as in ODT. Therefore, if the user needs to change any location, he should type the address followed by a slash (/) or back-slash (\), the monitor will then open that location just as in ODt. The user can roll up or down sequentially in memory by using the line feed or carat (^) keys. The SP0031 monitor is reentered from the ODT mode by typing a carriage return. Like ODT a memory location will only be modified if a valid octal number is typed before any of the ODT terminator characters. For example, to change the base and vector address of the DT2762 tests one would type:

542/177700 170400 (line-feed)

000544/000300 400 (return)

to change the base address to 170400 and vector address to 400. Note that this change is only temporary and the default addresses will be reloaded if the model number is retyped or if SP0031 is reloaded. In addition to these commands the SP0031 test executive allows the user to ask for the model directory, to start tests, to loop or halt on tests or even to reboot RT-11. The commands available to the user under the SP0031 test executive are listed on the following page.

Example: User wants to run a scope loop on Test 2 because an error is encountered. Type:

IL TEST (Space) 2

In this case the program will loop on Test 2 and inhibit error printouts.

If a test is run and no errors occur, the test will return to the SP0031 command level without any other messages. If however, an error does occur, then the test will print out the test number and error code. The user may look up the meaning of each error code in the program listings given in Appendix A.

10.4 Test Descriptions

All descriptions of the tests and the set up requirements needed for any particular test are described in detail in the program listings at the beginning of each test.

10.5 SP0031 Program Description

SP0031 consists of two groups of tests. The first group contains a series of tests which test all the logic of the interface board. These tests contain scope loops for debug purposes and will provide an error message if a problem exists. The second set of tests test the analog operation and calibration of the boards.

A listing of all the tests for testing DT2780 series boards can be found at the beginning of the program listings.

Note that the user can run all the logic tests by using the monitor ALL command. Calibration tests, however, must be run individually.

COMMAND	FUNCTION
ALL	Runs all logic tests that are present for current device. Generates an error if there is no current device.
BOOT	Jumps to the standard hardware bootstrap (173000). Generates an error if there is no bootstrap present.
DIRECTORY	Displays the contents of the current directory.
EXIT	Halts the processor
MODEL	Displays the parameters associated with the current device. Generates an error if there is no current device.
MODEL (Space) DTXXXX	Searches the current directory for the given model number. If found, makes that model the current device. Generates an error if there is no current directory or if the model number cannot be found.
TEST	Runs the last test executed.
TEST (Space) octal number	Runs the indicated test.

Test Command prefixes - The following command prefixes are to be

used with the TEST command to control the execution of the various tests.

COMMAND PREFIXES TO TEST EXECUTION COMMANDS

R	(TEST command only)	repeat this test continuously
L	(both TEST and ALL)	Loop on this test if an error is detected.
H	(both TEST and ALL)	halt test stream if an error is detected.
I	(both TEST and ALL)	inhibit error printout

Control-C will terminate any test.

Example: User wants to run a scope loop on Test 2 because an error is encountered. Type:

ILTEST (space) 2

In this case the program will loop on test 2 and inhibit error printouts.

SP0031 Error Codes - SP0031 will print an error code when a specific error is encountered. All codes are in the program listing and show the error and what test the program was in when a failure occured. Use the table of contents printed at the front of the listing to quickly find the lpages in the listing associated with the test that generates the error.

10.6 SP0031 Tests

Logic Tests:

Test 1: BRPLY from all registers
Test 2: Check ADCSR bits
Test 3: BINITL action
Test 4: Byte operation of ADCSR
Test 5: A/D Done bit and interrupt
Test 6: Error bit and interrupt
Test 7: End of logic tests
Calibration Initialization
Displays A/D Data
Test 10: A/D Calibration
Test 11: A/D Input channel scan
Test 12: A/D Input gain/channel scan
DAC Initialization
Test 13: A/D in to D/A out
Test 14: D/A ramps
Test 15: D/A calibration
Test 16: D/A square waves
Test 17: D/A out to A/D In

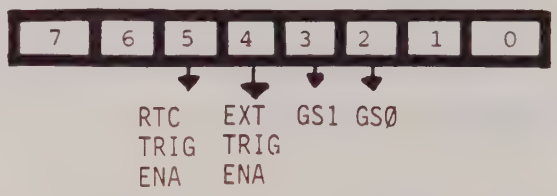
10.6.1 Test Description

All description of tests are located in the program listing at the beginning of each test.

10.6.2 Modes of Operation

Test 10, 11 and 12 will ask for a MODE input when they are called. This MODE input is the lower byte of the CSR.

When a user wants to run an interface under RTC control or EXT TRIG he can set these bits when the program asks for MODES. If a user wants to run under EXT TRIG he will set the MODES as 20_8. The GS0 and GS1 are bits to set the range for the PGX option.



MODE BITS FOR USE IN TEST 10, 11 AND 12.

10.6.3 Calibration

Calibration of the system requires a voltage standard for highly accurate analog inputs and a DVM for calibration of analog inputs. Note: User must calibrate ADC first, followed by the two D/A converters.

Equipment Required:

Voltage standard - EDC Model MV-100 or equivalent
- Data Technology Model 40 or equivalent.

10.6.3.1 Calibration of A/D Converter for DT2781/DT2785 (12 bit resolution)

Configuration: ±10V Full Scale, 2's complement notation.

1. Connect the voltage standard to CHØ input
2. Set voltage standard to -9.9976 volts
3. Start A/D calibration test (Test 10) for CHØ, Mode Ø.
4. Adjust A/D offset pot. for a printout flickering between 174000 and 174001.
5. Reset voltage standard to +9.9878 volts.
6. Adjust A/D range pot. for printout flickering between ØØ3777 and ØØ3776.

10.6.3.2 27xx/5714 A/D Calibration

Configuration ±10V FS, 2's Complement

1. Connect a voltage standard to CHØ
2. Set standard to -9.99939V
3. Start A/D calibration test (test 10) CHØ, mode Ø.
4. Adjust A/D offset for printout between 1ØØØØØ and 1ØØØ4 The two least significant bits are ignored.
5. Reset standard to + 9.9969
6. Adjust A/D range for printout between 7777Ø and 77774 (2 least significant bits ignored)

10.6.3.3 27xx/5716 A/D Calibration

1. Connect a voltage standard to CHØ.
2. Set standard to -9.99985V
3. Start A/D calibration test (test 10) CHØ, Mode Ø.
4. Adjust A/D offset for printout between 1 00000 and 100001
5. Reset standard to +9.99 24
6. Adjust A/D range for printout between 77777 and 77776.

10.6.3.4 D/A Calibration (Both Channels) Configuration 2's Complement Input

1. Connect lab quality DVM to DAC A out (pin 26). Ground DVM on DAC ret. (pin 25)
2. Start D/A calibration. (test 15)
3. Press space bar on terminal until approximately -10V is read on DVM.
4. Adjust zero pot.until exactly -10.0000V is read
5. Press space bar until +10V is read
6. Adjust range pot until +9.9951V is read
7. Repeat for DAC B

APPENDIX A

SOFTWARE DOCUMENTATION

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28- 925 Test 15: D/A Calibration
28- 950 Test 16: D/A Square waves
29- 969 Test 17: D/A out to A/D in

```
                        .LIST   TTM
                        .ENABL  LC
                        .TITLE  DT2781  TST-11 module
                        .IDENT  /V01 03/
000000                  .PSECT  DT2781
                .NLIST  BIN
        ;
        ;
                .SBTTL  General Information
        ;
        ;
        ; Copyright (C) 1979, Data Translation Incorporated. All
        ; rights reserved.No part of this program or publication
        ; may be reproduced without the prior written permission
        ; of  Data Translation Incorporated,  4 Strathmore Road,
        ; Natick, Mass. 01760.
        ;
        ;
        ; The information in this document is subject to change
        ; without  notice  and  should  not  be  construed as a
        ; commitment by Data Translation Incorporated.
        ;
        ;
        ; Data Translation cannot assume any responsibility for
        ; the use of any portion of this software for other than
        ; its intended  diagnostic  purpose  in calibrating and
        ; testing  Data  Translation  manufactured  analog  and
        ; digital interface boards.
        ;
        ;
        ;
        ; Version 01-03
        ;
        ;
        ;
        ;
        ;
        ;
        ; This program module contains routines to test and
        ; calibrate DTI DT2781 and DT2785  series analog
        ; interface systems for the LSI-11.  A complete listing
        ; of the models tested by this code module will be found
        ; on the following pages. This module is desioned to
        ; operate under TST-11 supervision
        ;
                        .LIST   BIN
```

```
                ;
                ;
                ;
                ;       The differences between V01-03 and V01-02 are.
                ;       1). Test 10 has been changed to accept odd numbered
                ;           channels
                ;
                ;       2). Self timing feature was added to time module
                ;           characteristics.
                ;
                ;
                ;       The differences between V01-02 and V01-01 are:
                ;       1). The timing in test 3 has been changed to
                ;           wait a full conversion time between triggers
                ;           befor the BINIT signal is cycled
                ;
                ;
                ;
                ;
                ,
                ;
                ;
                ;
                ;
```

```
                        .SBTTL  Test Parameter Block (TPB)
                ;
                ; Test-11 Declaration
                ;
                        .MCALL  TST11
                        TST11
                .LIST   ME
                ;
                ; EQUATED SYMBOLS
                ;
                ;       TERMINAL I/O PARAMETERS
                ;
 177560 RCSR    =177560         ; RECEIVER STATUS REGISTER
 177562 RBUF    =177562         ; RECEIVER DATA BUFFER
 177564 XCSR    =177564         ; TRANSMITTER STATUS REGISTER
 177566 XBUF    =177566         ; TRANSMITTER DATA BUFFER
                ;
                ;       SPECIAL ASCII CHARACTERS
                ;
 000003 CTRLC   =3              ; CONTROL-C
 000012 LF      =12             ; LINE FEED
 000014 FF      =14             ; FORM FEED
 000015 CR      =15             ; CARRIAGE RETURN
 000040 SPACE   =40             ; SPACE CODE
 000011 CTRLI   =11             ; CONTROL-I (TAB)
 000177 DEL     =177            ; DELETE CODE
                ;
                ;
                ; PRIORITY 7 PSW
 000340 PR7     =340
                ;
                ; BIT DEFINITIONS
                ;
 100000 BIT15   =100000
 040000 BIT14   =40000
 020000 BIT13   =20000
 010000 BIT12   =10000
 004000 BIT11   =4000
 002000 BIT10   =2000
 001000 BIT9    =1000
 000400 BIT8    =400
 000200 BIT7    =200
 000100 BIT6    =100
 000040 BIT5    =40
 000020 BIT4    =20
 000010 BIT3    =10
 000004 BIT2    =4
 000002 BIT1    =2
 000001 BIT0    =1
```

```
                        ; TST-11 PARAMETER STORAGE
                        ;
                        ;
                000514  ODTACC  =514    ; ODT ACCUMULATOR
                000526  ERRCNT  =526    ; # OF ERRORS
                        ;
                        ;
                        ; PARAMETER STORAGE FOR CODE MODULES
                        ;
                000540  SWR     =540    ; SWITCH REGISTER
                000542  BASE    =542    ; BASE ADDRESS
                000544  VECTOR  =544    ; VECTOR ADDRESS
                000546  DELAY   =546    ; DELAY COUNT
                        ;
     80                 ;
     81                 ;
     82                 ; Additional parameters used by this diagnostic
     83                 ;
     84                 ;
     85         000546  DELAY   =546            ; A/D delay count storage
     86
     87         000522  ERRCNT  =522            ; error counter
     88                 ;
     89                 ;
     90                 ; Test Parameter Block
     91                 ;
     92                 .NLIST  BIN
     93         ;
     94 000000  TPB:     .WORD   PARAM           ; address of parameter
     95                                         ; print-out routine
     96 000002          .BYTE   377             ; reserved
     97 000003          .BYTE   17              ; # of tests
     98         ;
     99         ; Test Address Table for use by TST-11
    100         ;
    101 000004          .WORD   TEST1,PR7
    102 000010          .WORD   TEST2,PR7
    103 000014          .WORD   TEST3,PR7
    104 000020          .WORD   TEST4,PR7
    105 000024          .WORD   TEST5,PR7
    106 000030          .WORD   TEST6,PR7
    107 000034          .WORD   TEST7,PR7
    108 000040          .WORD   TEST10,0
    109 000044          .WORD   TEST11,0
    110 000050          .WORD   TEST12,0
    111 000054          .WORD   TEST13,0
    112 000060          .WORD   TEST14,0
    113 000064          .WORD   TEST15,0
    114 000070          .WORD   TEST16,0
    115 000074          .WORD   TEST17,0
    116         ;
    117                         .LIST   BIN
```

INITIALIZATION

```
                                .SBTTL  Initialization
                        ;
000100  005037  INIT:   CLR     @#SWR           ; input only model
        000540
000104  012737          MOV     #0,@#DELAY      ; init delay
        000000
        000546
000112                  RELMOV  #CHNL,R1        ; check SE or DI
000112  010701          MOV     PC,R1           ; MOVE PC TO R1
000114  062701          ADD     #CHNL-.,R1      ; ADD IN RUN-TIME OFFSET
        000271
000120  004767          CALL    QUERY
        000074
000124  103407          BCS     1$              ; is SE
000126                  SET     BIT6,SWR        ; is DI
000126  052737          BIS     #<BIT6>,@#SWR
        000100
        000540
000134  012737          MOV     #20,@#ODTACC    ; set channel number
        000020
        000514
000142  000403          BR      2$
                        ;
000144  012737  1$:     MOV     #10,@#ODTACC    ; set channel number
        000010
        000514
000152          2$:     RELMOV  #DACTYP,R1      ; check dac type
000152  010701          MOV     PC,R1           ; MOVE PC TO R1
000154  062701          ADD     #DACTYP-.,R1    ; ADD IN RUN-TIME OFFSET
        000211
000160  004767          CALL    QUERY
        000034
000164  103403          BCS     3$              ; dac is offset binary
000166                  SET     BIT7,SWR        ; dac is 2's complement
000166  052737          BIS     #<BIT7>,@#SWR
        000200
        000540
000174  113737  3$:     MOVB    @#ODTACC,@#SWR+1
        000514
        000541
000202  012737          MOV     #170400,@#BASE  ; set default address
        170400
        000542
000210  012737          MOV     #400,@#VECTOR   ; set default vector
        000400
        000544
000216  000207          RETURN                  ; all done
```

```
140 000220            QUERY:  PUSH    R1              ; save pointer
141 000222                    PRINTS                  ; print prompt
142 000224                    PRINT   <(Y or N)? >
143 000242                    TTYIN
144 000244  122700            CMPB    #'Y,R0          ; a "Y"?
            000131
145 000250  001427            BEQ     2$
146 000252  122700            CMPB    #'N,R0          ; a "N"?
            000116
147 000256  001422            BEQ     1$              ; yes
148 000260                    CRLF
149 000262                    PRINTC  <See manual for assistance >
150 000320                    POP     R1              ; restore pointer
151 000322  000736            BR      QUERY
152                     ;
153 000324  000261    1$:     SEC                     ; set carry flag
154 000326  000401            BR      3$
155 000330  000241    2$:     CLC                     ; clear carry flag
156 000332            3$:     TTYOUT                  ; echo character
157 000334                    CRLF
158 000336                    POP     R1              ; restore R1
159 000340  000207            RETURN
160                     ;
161                     ;
162                     .NLIST  BIN
163 000342  SPEED:    .ASCIZ  "100 KHz A/D module"
164 000365  DACTYP:   .ASCIZ  "2'S COMPLEMENT "
165 000405  CHNL:     .ASCIZ  "IS BOARD SE "
166                     .EVEN
167                             .LIST   BIN
168                     ,
169                     ,
170                     ;
171                             .SBTTL  Display Parameters
172                     ;
173                     ;       This routine displays the current setting
174                     ;       of 'BASE' and 'VECTOR' on the system console
175                     ;       terminal.
176                     ,
177 000422            PARAM:  PRINT   <Base address =
178 000444  013700            MOV     @#BASE,R0       ; get base address
            000542
179 000450                    OCT16                   ; display
180 000452                    CRLF
181 000454                    PRINT   <Vector address =
182 000500  013700            MOV     @#VECTOR,R0     ; get vector address
            000544
183 000504                    OCT16                   ; display
184 000506                    CRLF
185 000510  000207            RETURN                  ; all done
```

```
                        .SBTTL  Error reporters
                ;
                ;
                ; This routine provides error reporting for bus
                ; time-out errors (no BRPLY from interface)
                ;
000512          NORPLY: PRINT   <No BRPLY when accessing location >
000556  010100          MOV     R1,R0
000560                  OCT16                   ; display address
000562                  CRLF
000564  000207          RETURN                  ; done
                ;
                ;
                ; This routine provides error reporting for register
                ; bit errors (one or more incorrect bits in a register)
                ;
000566          REG:    PRINTC  <Register Error:
000610                  PRINT   <Address: >
000624                  PUSH    R0              ; save R0
000626  010100          MOV     R1,R0           ; get address
000630                  OCT16
000632                  CRLF
000634                  PRINT   <Expected:>
000650  010200          MOV     R2,R0           ; get expected value
000652                  OCT16                   ; display
000654                  CRLF
000656                  PRINT   <Found:    >
000672  011600          MOV     (SP),R0         ; get bad bits
000674  074200          XOR     R2,R0           ; generate snapshot
000676                  OCT16                   ; display
000700                  CRLF                    ; formatting
000702                  PRINT   <Bits:     >
000716                  POP     R0              ; get error bits
000720                  OCT16                   ; display
000722                  CRLF
000724  000207          RETURN                  ; done
```

```
                        .SBTTL  Model testing information
                .NLIST  BIN
        ;
        ; This code module contains the routines necessary
        ; to test the following DTI interface models
        ;
        ;
        ;
        ;       DT2781  High level analog input
        I2781   ==INIT
        T2781   ==TPB
        ;
        ;
        ;       DT2785  Wide range analog input
        I2785   ==INIT
        T2785   = TPB
        ;
        ;
        ;
                        .LIST   BIN
                ;
                ;
                ; Software switch register bit reservations
                ;
                ; bits 14-15:   not used
                ; bits 13-8:    # of A/D channels
                ; bit 7:        2's complement
                ; bit 6:        DI module present
                ; bits 3-5:     not used
                ; bits 2-0:     reserved
```

```
                        .SBTTL  Logic Tests
                        .SBTTL  Test 1.  BRPLY from all registers
                ;
                ; This test verifies that the interface system responds
                ; with a bus reply signal during a bus DATIO bus cycle
                ; All registers available on the board are checked
                ;
                ;
000726  010602  TEST1:  MOV     SP,R2           ; save SP
000730                  RELMOV  #2$,R0          ; set up trap to 4
000730  010700          MOV     PC,R0           ; MOVE PC TO R0
000732  062700          ADD     #2$-.,R0        ; ADD IN RUN-TIME OFFSET
        000060
000736  010037          MOV     R0,@#4
        000004
000742  013701  1$:     MOV     @#BASE,R1       ; get address
        000542
000746                  SCOPE                   ; declare loop point
000750  005011          CLR     (R1)            ; DATIO bus cycle
000752                  SCOPE                   ; declare loop point
000754  062701          ADD     #2,R1           ; next register
        000002
000760                  SCOPE                   ; declare loop point
000762  005011          CLR     (R1)            ; DATIO bus cycle
000764                  SCOPE                   ; declare loop point
000766  062701          ADD     #2,R1           ; next register
        000002
000772                  SCOPE                   ; declare loop point
000774  005011          CLR     (R1)            ; DATIO bus cycle
000776                  SCOPE                   ; declare loop point
001000  062701          ADD     #2,R1           ; next register
        000002
001004                  SCOPE                   ; declare loop point
001006  005011          CLR     (R1)            ; DATIO bus cycle
001010                  EXIT
                ;
                ; ****************************************************
                ;
                ;       Error Code 1 - Bus timeout
                ;
                ; ****************************************************
                ;
001012  011603  2$:     MOV     (SP),R3         ; get offending PC
001014  010206          MOV     R2,SP           ; restore stack
001016                  ERROR   1,NORPLY        ; report error
001022  000113          JMP     (R3)            ; continue test
```

```
                        .SBTTL  Test 2:  check ADCSR bits
                ;
                ; This test checks most of the bits in ADCSR
                ; Bits are checked for both set and reset capability
                ; The bit that is NOT checked is the A/D DONE bit
                ; it is checked in other tests.
                ;
001024 013701   TEST2:  MOV     @#BASE,R1       ; get address
       000542
001030 005002           CLR     R2              ; init test reg
001032 012703           MOV     #40,R3          ; set # of states
       000040
001036                  SCOPE                   ; declare loop point
001040 010211   1$:     MOV     R2,(R1)         ; set bits
001042 013704           MOV     @#DELAY,R4      ; set counter
       000546
001046 077401   2$:     SOB     R4,2$           ; delay for setteling
001050 011100           MOV     (R1),R0         ; get bits
001052 042700           BIC     #177600,R0      ; ignore high byte
       177600
001056 074200           XOR     R2,R0           ; test bits
001060 001402           BEQ     3$              ; no error - skip
                ;
                ; ****************************************
                ;
                ;       Error Code 2 - bit error, ADCSR
                ;                      bits 0-6
                ;
                ; ****************************************
                ;
001062                  ERROR   2,REG           ; report error
                ;
001066 062702   3$:     ADD     #4,R2           ; next state
       000004
001072 077316           SOB     R3,1$           ; loop until done
001074 005002           CLR     R2              ; init test reg
001076 012703           MOV     #16,R3          ; set # of states
       000016
001102                  SCOPE                   ; declare loop point
001104 010211   4$:     MOV     R2,(R1)         ; set bits
001106 013704           MOV     @#DELAY,R4      ; set counter
       000546
001112 077401   5$:     SOB     R4,5$           ; delay
001114 011100           MOV     (R1),R0         ; get bits
001116 042700           BIC     #170377,R0      ; ignore low byte
       170377
001122 074200           XOR     R2,R0           ; test bits
001124 001402           BEQ     6$              ; no error - skip
                ;
```

TEST 2 CHECK ADCSR BITS

```
                        ;
                        ; ***********************************************
                        ;
                        ;       Error Code 3 - bit error, ADCSR
                        ;                      bits 8-11
                        ;
                        ; ***********************************************
                        ;
001126                  ERROR   3,REG           ; report error
                        ;
001132  062702  6$:     ADD     #400,R2         ; next state
        000400
001136  077316          SOB     R3,4$           ; loop until done
001140  005002          CLR     R2
001142  012703          MOV     #4,R3           ; set number of states
        000004
001146                  SCOPE
001150  010211  7$:     MOV     R2,(R1)         ; set bits
001152  013704          MOV     @#DELAY,R4      ; set counter
        000546
001156  077401  8$:     SOB     R4,8$           ; wait to finish
001160  011100          MOV     (R1),R0         ; get bits
001162  042700          BIC     #37777,R0       ; ignore some bits
        037777
001166  074200          XOR     R2,R0           ; test bits
001170  001402          BEQ     9$              ; no error skip
                        ;
                        ; ***********************************************
                        ;
                        ;       ERROR CODE 4 - bit error ADCSR
                        ;                      bits 14 and 15
                        ;
                        ; ***********************************************
                        ;
001172                  ERROR   4,REG           ; report error
                        ;
001176  062702  9$:     ADD     #40000,R2       ; next state
        040000
001202  077316          SOB     R3,7$           ; loop till done
001204                  EXIT
```

```
                        .SBTTL  Test 3   BINITL action
                ;
                ; This test verifies that the BINITL signal clears
                ; the proper ADCSR bits
                ;
                ;
001206  013701  TEST3:  MOV     @#BASE,R1       ; get address
        000542
001212  012711          MOV     #40101,(R1)     ; set bits
        040101
001216  013700          MOV     @#DELAY,R0      ; wait for A/D DONE
        000546
001222  077001  1$:     SOB     R0,1$
001224  105211          INCB    (R1)            ; set error bit
001226  005002          CLR     R2              ; clr test reg.
001230                  SCOPE                   ; declare loop point
001232  013700          MOV     @#DELAY,R0      ; wait for A/D DONE
        000546
001236  077001  2$:     SOB     R0,2$
001240  000005          RESET                   ; issue BINITL
001242  011100          MOV     (R1),R0         ; get bits
001244  042700          BIC     #37476,R0       ; ignore some bits
        037476
001250  074200          XOR     R2,R0           ; test bits
001252  001402          BEQ     3$              ; OK - skip error
                ;
                ; ****************************************
                ;
                ;       Error code 5 - proper bit(s) not cleared
                ;                       by BINITL
                ;
                ; ****************************************
                ;
001254                  ERROR   5,REG           ; report error
                ;
001260          3$:     EXIT                    ; all done
```

```
                        .SBTTL  Test 4:  byte operation of ADCSR
                ;
                ; This test verifies high and low byte operations
                ; involving the ADCSR
                ;
001262 013701   TEST4:  MOV     @#BASE,R1       ; get address
       000542
001266 005011           CLR     (R1)            ; clear ADCSR
001270 005002           CLR     R2              ; init. test register
001272                  SCOPE                   ; declare loop point
001274 112711           MOVB    #-1,(R1)        ; set R/W bits
       177777
001300 013705           MOV     @#DELAY,R5      ; wait to settle
       000546
001304 077501   1$:     SOB     R5,1$
001306 011100           MOV     (R1),R0         ; get ADCSR as word
001310 042700           BIC     #100377,R0      ; ignore low byte
       100377
001314 074200           XOR     R2,R0           ; test bits
001316 001402           BEQ     2$              ; ok - skip error
                ;
                ; ***************************************
                ;
                ;       Error Code 6 - high byte loaded during
                ;                       a low byte operation
                ;
                ; ***************************************
                ;
001320                  ERROR   6,REG           ; report error
                ;
001321 005011   2$:     CLR     (R1)            ; clear ADCSR
001326 005002           CLR     R2              ; init. test register
001330 005201           INC     R1              ; point to high byte
001332                  SCOPE                   ; declare loop point
001334 013705           MOV     @#DELAY,R5      ; wait to settle
       000546
001340 077501   3$:     SOB     R5,3$
001342 112711           MOVB    #-1,(R1)        ; set R/W bits
       177777
001346 016100           MOV     -1(R1),R0       ; get ADCSR as word
       177777
001352 042700           BIC     #177600,R0      ; ignore high byte
       177600
001356 074200           XOR     R2,R0           ; test bits
001360 001402           BEQ     4$              ; ok - skip error
                ;
                ; ***************************************
                ;
                ;       Error Code 7 - low byte loaded during
                ;                       a high byte operation
                ;
                ; ***************************************
                ;
001362                  ERROR   7,REG           ; report error
```

```
                                SBTTL  Test 5:  A/D DONE bit and interrupt
                        ;
                        ; This test verifies that the A/D DONE bit can
                        ; be set properly and that the INT ENB bit
                        ; functions properly
                        ;
                        ;
001370  013701  TEST5:  MOV     @#BASE,R1       ; get address
        000542
001374  013702          MOV     @#VECTOR,R2     ; get vector address
        000544
001400  005761          TST     2(R1)           ; clear A/D DONE bit
        000002
001404  005011          CLR     (R1)            ; clear ADCSR
001406                  SCOPE                   ; declare loop point
001410  105211          INCB    (R1)            ; set A/D DONE bit
001412  013700          MOV     @#DELAY,R0      ; wait for A/D DONE
        000546
001416  077001  1$:     SOB     R0,1$
001420  105711          TSTB    (R1)            ; is bit set?
001422  100402          BMI     2$              ; yes - skip error
                        ;
                        ; ***************************************
                        ;
                        ;       Error Code 10 - A/D DONE bit not set
                        ;
                        ; ***************************************
                        ;
001424                  ERROR   10              ; report error
001426  000505          BR      14$             ; can't continue
                        ;
001430          2$:     SCOPE                   ; declare loop point
001432  005761          TST     2(R1)           ; read ADDBR
        000002
001436  105711          TSTB    (R1)            ; done bit clear?
001440  100002          BPL     3$              ; yes - skip error
                        ;
                        ; ***************************************
                        ;
                        ;       Error Code 11 - A/D DONE bit not cleared
                        ;                       after A/D data was read
                        ;
                        ; ***************************************
                        ;
001442                  ERROR   11              ; report error
001444  000476          BR      14$             ; can't continue
```

```
497 001446  005003  3$:     CLR     R3              ; prepare status words
498 001450  012704          MOV     #PR7,R4
            000340
499 001454                  RELMOV  #5$,R0          ; get ISR address
    001454  010700          MOV     PC,R0           ; MOVE PC TO R0
    001456  062700          ADD     #5$-.,R0        ; ADD IN RUN-TIME OFFSET
            000042
500 001462  010012          MOV     R0,(R2)         ; store
501 001464  010462          MOV     R4,2(R2)        ; store status too
            000002
502 001470                  SCOPE                   ; declare loop point
503 001472  105211          INCB    (R1)            ; set A/D DONE
504 001474  013700          MOV     @#DELAY,R0      ; wait for DONE
            000546
505 001500  077001  4$:     SOB     R0,4$
506 001502  052711          BIS     #100,(R1)       ; enable interrupts
            000100
507 001506  106403          MTPS    R3              ; enable CPU interrupts
508 001510  000240          NOP                     ; stall time
509 001512  106404          MTPS    R4              ; turn off CPU
510                 ;
511                 ; ***************************************************
512                 ;
513                 ;       Error Code 12 - no interrupt on A/D DONE
514                 ;
515                 ; ***************************************************
516                 ;
517 001514                  ERROR   12              ; report error
518 001516  000451          BR      14$             ; can't continue
519                 ;
520 001520  062706  5$:     ADD     #4,SP           ; adjust stack
            000004
521 001524                  SCOPE                   ; declare loop point
522 001526  005761          TST     2(R1)           ; read ADDBR
            000002
523 001532  105711          TSTB    (R1)            ; A/D DONE clear?
524 001534  100002          BPL     6$              ; yes - exit
525                 ;
526                 ; ***************************************************
527                 ;
528                 ;       Error Code 13 - A/D DONE bit not cleared
529                 ;                       after A/D data was read
530                 ;
531                 ; ***************************************************
532                 ;
533 001536                  ERROR   13              ; report error
534 001540  000440          BR      14$             ; can't continue
```

```
536 001542          6$:     SCOPE                   ; declare loop point
537 001544 005761           TST     2(R1)           ; clear DONE
           000002
538 001550 005011           CLR     (R1)            ; clear ADCSR
539 001552 005211           INC     (R1)            ; start conversion
540 001554 105711   7$:     TSTB    (R1)            ; wait for done
541 001556 100376           BPL     7$
542 001560 005711           TST     (R1)            ; error bit set?
543 001562 100001           BPL     8$              ; no - exit
544                 ;
545                 ; ***************************************
546                 ;
547                 ;       Error Code 14 - Error bit set after normal
548                 ;                       A/D triggering sequence
549                 ;
550                 ; ***************************************
551                 ;
552 001564                  ERROR   14              ; report error
553                 ;
554 001566 005761   8$:     TST     2(R1)           ; clear DONE
           000002
555                 ;
556                 ;       Board cycles compute time delay for A/D
557                 ;
558 001572 005011   9$:     CLR     (R1)            ; clear CSR
559 001574 005000           CLR     R0              ; clear counter
560 001576 013702           MOV     @#DELAY,R2      ; wait to settle
           000546
561 001602 001017           BNE     14$             ; leave if non zero
562 001604 077201   10$:    SOB     R2,10$
563 001606 005211           INC     (R1)            ; start conversion
564 001610 005200   11$:    INC     R0              ; bump counter
565 001612 103407           BCS     12$             ; leave if overflow
566 001614 105711           TSTB    (R1)            ; wait for done
567 001616 100374           BPL     11$             ; no done
568 001620 006300           ASL     R0              ; multiply by 16
569 001622 006300           ASL     R0              ; create new delay
570 001624 006300           ASL     R0              ; create new delay
571 001626 006300           ASL     R0              ; create new delay
572 001630 102002           BVC     13$             ; branch if no overflow
573 001632 012700   12$:    MOV     #-1,R0          ; force max delay -1
           177777
574 001636 010037   13$:    MOV     R0,@#DELAY      ; store it
           000546
575 001642 005761   14$:    TST     2(R1)           ; clear done
           000002
576 001646 005011           CLR     (R1)            ; clear CSR
577 001650                  EXIT                    ; leave
578                 ;
```

```
                        .SBTTL  Test 6.  ERROR bit and interrupt
                ;
                ; This test verifies that the ERROR bit can be set
                ; properly and that the ERR INT ENB bit functions
                ; correctly
                ;
                ;
001652  013701  TEST6:  MOV     @#BASE,R1       ; get address
        000542
001656  013702          MOV     @#VECTOR,R2     ; get vector address
        000544
001662  062702          ADD     #4,R2           ; adjust vertor
        000004
001666  005761          TST     2(R1)           ; clear A/D DONE bit
        000002
001672                  SCOPE                   ; declare loop point
001674  005011          CLR     (R1)            ; clear ADCSR
001676  005711          TST     (R1)            ; ERROR clear?
001700  100002          BPL     1$              ; yes - skip error
                ;
                ; ********************************************
                ;
                ;       Error Code 15 - ERROR bit not clear
                ;
                ; ********************************************
                ;
001702                  ERROR   15              ; report error
001704  000441          BR      5$              ; can't continue
                ;
001706          1$:     SCOPE                   ; declare loop point
001710  105211          INCB    (R1)            ; set A/D DONE bit
001712  105711  2$:     TSTB    (R1)            ; test for done
001714  100376          BPL     2$              ; wait for done
001716  105211          INCB    (R1)            ; set error bit
001720  005711          TST     (R1)            ; is bit set?
001722  100402          BMI     3$              ; yes - skip error
                ;
                ; ********************************************
                ;
                ;       Error Code 16 - ERROR bit not set
                ;
                ; ********************************************
                ;
001724                  ERROR   16              ; report error
001726  000430          BR      5$              ; can't continue
```

```
                622 001730  005003  3$:     CLR     R3              ; prepare status words
                623 001732  012704          MOV     #PR7,R4
                            000340
                624 001736                  RELMOV  #4$,R0          ; get ISR address
                    001736  010700          MOV     PC,R0           ; MOVE PC TO R0
                    001740  062700          ADD     #4$-.,R0        ; ADD IN RUN-TIME OFFSET
                            000032
                625 001744  010012          MOV     R0,(R2)         ; store
                626 001746  010462          MOV     R4,2(R2)        ; store status too
                            000002
                627 001752                  SCOPE                   ; declare loop point
                628 001754  052711          BIS     #40000,(R1)     ; enable interrupts
                            040000
                629 001760  106403          MTPS    R3              ; enable CPU interrupts
                630 001762  000240          NOP                     ; stall time
                631 001764  106404          MTPS    R4              ; turn off CPU
                632                 ;
                633                 ; ********************************************
                634                 ;
                635                 ;       Error Code 17 - no interrupt on ERROR
                636                 ;
                637                 ; ********************************************
                638                 ;
                639 001766                  ERROR   17              ; report error
                640 001770  000407          BR      5$              ; can't continue
                641                 ;
                642 001772  062706  4$:     ADD     #4,SP           ; adjust stack
                            000004
                643 001776                  SCOPE                   ; declare loop point
                644 002000  005011          CLR     (R1)            ; clear ERROR bit
                645 002002  005711          TST     (R1)            ; check bit
                646 002004  100001          BPL     5$              ; clear - skip error
                647                 ;
                648                 ; ********************************************
                649                 ;
                650                 ;       Error Code 20 - ERROR bit not clear
                651                 ;
                652                 ; ********************************************
                653                 ;
                654 002006                  ERROR   20              ; report error
                655                 ;
                656 002010  005761  5$:     TST     2(R1)           ; clear DONE
                            000002
                657 002014  005011          CLR     (R1)            ; clear ADCSR
                658 002016                  EXIT
```

```
                        .SBTTL  Test 7:  End of logic tests
                ;
                ; This test is present to inform the TST-11 monitor
                ; that there are no more additional logic tests
                ; to be executed. When the "ALL" command is used,
                ; this test will force a return to the command
                ; level of TST-11 when the test sequencer reaches
                ; this test.
                ;
                ;
002020          TEST7:  ESCAPE
                ;
                ;
                        .SBTTL  Calibration initialization
                ;
                ; This routine performs initialization functions
                ; for some of the calibration tests
                ;
                ;
002022          GETCH:  PRINT   <Channel? >      ; output prompt
002036                  GETOCT                   ; get value
002040  103422          BCS     1$               ; CR at end - cont
002042                  PRINTC  <Enter an octal channel address >
002104  000746          BR      GETCH            ; try again
                ;
002106  013701  1$:     MOV     @#BASE,R1        ; get address
        000542
002112  013702          MOV     @#ODTACC,R2      ; get value
        000514
002116  000302          SWAB    R2               ; adjust
002120          2$:     PRINT   <Mode bits? >    ; output prompt
002136                  GETOCT                   ; get value
002140  103420          BCS     3$               ; CR at end - cont
002142                  PRINTC  <Enter an octal byte value.>
002200  000747          BR      2$
                ;
002202  042702  3$:     BIC     #377,R2          ; clear low byte,R2
        000377
002206  013700          MOV     @#ODTACC,R0      ; get value
        000514
002212  042700          BIC     #177400,R0       ; clear high byte,R0
        177400
002216  060002          ADD     R0,R2            ; add in mode byte
002220  005761          TST     2(R1)            ; clear DONE
        000002
002224  005011          CLR     (R1)             ; clear board
002226  000207          RETURN
```

DISPLAY A/D DATA

```
                        .SBTTL  Display A/D data
                ;
                ; This routine takes the data from ADUBR and displays
                ; it for the user as a 16 bit octal value
                ;
002230  016100  DISPLY: MOV     2(R1),R0        ; get data
        000002
002234                  OCT16                   ; print
002236  005711          TST     (R1)            ; error bit set?
002240  100015          BPL     1$              ; no - return
002242  112700          MOVB    #'E,R0          ; print 'E'
        000105
002246                  TTYOUT
002250  042711          BIC     #40000,(R1)     ; clear error bit
        040000
002254  005237          INC     @#ERRCNT        ; inc. count
        000522
002260  005737          TST     @#ERRCNT        ; overflow?
        000522
002264  001003          BNE     1$              ; no - skip
002266  012737          MOV     #-1,@#ERRCNT    ; yes - force value
        177777
        000522
002274  000207  1$:     RETURN
                ;
                ;
                        .SBTTL  Test 10: A/D Calibration
                ;
                ; This test accepts a channel address from the user
                ; and displays the data from that channel continuously.
                ;
                ;
002276          TEST10: PRINTC  <A/D Calibration>
002320  004767          CALL    GETCH           ; get channel address
        177476
002324                  KBEXIT                  ; set up keyboard
002326  042702          BIC     #140303,R2      ; clear some bits
        140303
002332  032702          BIT     #60,R2          ; external?
        000060
002336  001002          BNE     1$              ; yes - no start bit
002340  052702          BIS     #1,R2           ; set start bit
        000001
002344  112704  1$:     MOVB    #10,R4          ; line counter
        000010
002350                  CRLF
002352  010211  2$      MOV     R2,(R1)         ; start conversion
002354  105711  3$      TSTB    (R1)            ; wait for DONE
002356  100376          BPL     3$
002360  004767          CALL    DISPLY          ; display data
        177644
002364  105304          DECB    R4              ; line over?
002366  001766          BEQ     1$              ; yes - new line
002370                  TYI
002372  000765          BR      2$              ; next conversion
```

```
                        .SBTTL  Test 11: A/D input channel scan
                ;
                ; This test scans the input channels while
                ; displaying the A/D data on the terminal.
                ;
                ;
002374          TEST11: PRINTC  <A/D Input channel scan>
002426                  KBEXIT                  ; set up keyboard
002430  013701          MOV     @#BASE,R1       ; get address
        000542
002434  005761          TST     2(R1)           ; clear DONE
        000002
002440  005011          CLR     (R1)            ; clear CSR
002442  005002          CLR     R2              ; init. channel count
002444          1$:     CRLF
002446  112703          MOVB    #10,R3          ; line counter
        000010
002452                  PRINT   <CH=>           ; display address
002460  010200          MOV     R2,R0
002462                  OCT8
002464  010200          MOV     R2,R0           ; get channel address
002466  000300          SWAB    R0              ; put in high byte
002470  010011          MOV     R0,(R1)         ; set up channel
002472  013700          MOV     @#DELAY,R0      ; wait to settle
        000546
002476  077001  2$:     SOB     R0,2$
002500  105211  3$:     INCB    (R1)            ; trigger converter
002502  105711  4$:     TSTB    (R1)            ; wait for DONE
002504  100376          BPL     4$
002506                  TAB
002510  004767          CALL    DISPLY          ; display data
        177514
002514  105303          DECB    R3              ; line done?
002516  001370          BNE     3$              ; no - continue
002520  005202          INC     R2              ; inc. channel
002522  123702          CMPB    @#SWR+1,R2      ; end of range?
        000541
002526  001346          BNE     1$              ; no - continue
002530  005002          CLR     R2              ; yes
002532                  CRLF
002534  000743          BR      1$
```

```
                        .SBTTL  Test 12: A/D input gain/channel scan
                ;
                ; This test scans the input channels while
                ; changing the gain of the converter.  The
                ; A/D data is displayed on the terminal.
                ;
                ;
002536          TEST12: PRINTC  <A/D Input gain/channel scan>
002574                  KBEXIT                  ; set up keyboard
002576  013701          MOV     @#BASE,R1       ; get address
        000542
002602  005761          TST     2(R1)           ; clear DONE
        000002
002606  005011          CLR     (R1)            ; clear CSR
002610  005002          CLR     R2              ; init. channel count
002612  005003          CLR     R3              ; init. gain
002614          1$:     CRLF
002616  112704          MOVB    #7,R4           ; line counter
        000007
002622                  PRINT   <CH=>           ; display address
002630  010200          MOV     R2,R0
002632                  OCTB
002634  112700          MOVB    #',,R0          ; display gain
        000054
002640                  TTYOUT
002642  112700          MOVB    #'0,R0
        000060
002646  032703          BIT     #10,R3          ; GS1 set?
        000010
002652  001401          BEQ     2$              ; no - skip
002654  105200          INCB    R0
002656          2$:     TTYOUT                  ; display bit
002660  112700          MOVB    #'0,R0
        000060
002664  032703          BIT     #4,R3           ; GS0 set?
        000004
002670  001401          BEQ     3$              ; no - skip
002672  105200          INCB    R0
002674          3$:     TTYOUT                  ; display bit
```

```
813 002676  010200          MOV     R2,R0           ; get channel address
814 002700  000300          SWAB    R0              ; put in high byte
815 002702  050300          BIS     R3,R0           ; set gain bits
816 002704  010011          MOV     R0,(R1)         ; set up channel
817 002706  105211  4$:     INCB    (R1)            ; trigger converter
818 002710  105711  5$:     TSTB    (R1)            ; wait for DONE
819 002712  100376          BPL     5$
820 002714                  TAB
821 002716  004767          CALL    DISPLY          ; display data
                177306
822 002722  105304          DECB    R4              ; line done?
823 002724  001370          BNE     4$              ; no - continue
824 002726  005202          INC     R2              ; inc. channel
825 002730  062703          ADD     #4,R3           ; increment gain
                000004
826 002734  042703          BIC     #177763,R3      ; clear extra bits
                177763
827 002740  123702          CMPB    @#SWR+1,R2      ; end of range?
                000541
828 002744  001323          BNE     1$              ; no - continue
829 002746  005002          CLR     R2              ; yes
830 002750                  CRLF
831 002752  000720          BR      1$
832                 ;
```

```
                        .SBTTL  DAC initialization
                ;
                ; This routine provides initialization functions
                ; for some of the tests that exercise the DACs
                ;
                ;
002754 012703   DAC:    MOV     #4000,R3        ; load -fs value
       004000
002760 074505           XOR     R5,R5           ; make zero value
002762 012704           MOV     #3777,R4        ; load +fs value
       003777
                ;
                ; data is now all set for two's comp
                ;
002766                  TEST    BIT7,SWR        ; check for offset binary?
002766 032737           BIT     #<BIT7>,@#SWR
       000200
       000540
002774 001003           BNE     1$              ; data form ok- continue on
                ;
                ; make values for offset binary
                ;
002776 010305           MOV     R3,R5           ; form zero value
003000 050304           BIS     R3,R4           ; form +fs value
003002 074303           XOR     R3,R3           ; form -fs value
                ;
003004 013701   1$:     MOV     @#BASE,R1       ; get base address
       000542
003010 062701           ADD     #4,R1           ; form dac A address
       000004
003014 010102           MOV     R1,R2
003016 062702           ADD     #2,R2           ; form dac B address
       000002
003022 000207           RETURN
                ;
                ;       This routine allows time for dacs A and B
                ;       to settle
                ;
003024          TIME:   PUSH    R0              ; save R0 for later
003026 012700           MOV     #20,R0          ; set delay
       000020
003032 077001   1$:     SOB     R0,1$           ; wait
003034                  POP     R0              ; restore R0
003036 000207           RETURN
                ;
```

```
                        .SBTTL  Test 13  A/D in to D/A out
                ;
                ; This test allows a user to connect a signal source
                ; to input channel 0 and see what should be the
                ; same signal appearing on the A DAC output.
                ;
                ;
003040  004767  TEST13: CALL    DAC
        177710
003044                  PRINTC  <Connect signal source to channel 0>
003112                  KBEXIT                  ; set up keyboard
003114  013701          MOV     @#BASE,R1       ; get address
        000542
003120  005761          TST     2(R1)           ; clear DONE
        000002
003124  005011          CLR     (R1)            ; start loop
003126  105211          INCB    (R1)
003130  105711  1$:     TSTB    (R1)            ; wait for DONE
003132  100376          BPL     1$
003134  016100          MOV     2(R1),R0        ; get data
        000002
003140  105211          INCB    (R1)            ; start next conversion
003142  042700          BIC     #170000,R0      ; prepare A DAC data
        170000
003146  010061          MOV     R0,4(R1)        ; load DAC data
        000004
003152  004767          CALL    TIME            ; wait for dac to settle
        177646
003156  000764          BR      1$
```

```
                        .SBTTL  Test 14: D/A Ramps
                ;
                ; This test generates rising and falling
                ; ramps on the DAC outputs
                ;
                ;
003160 004767   TEST14: CALL    DAC             ; init. DACs
       177570
003164                  PRINTC  <D/A Ramps>
003200                  KBEXIT                  ; set up keyboard
003202 012705   1$:     MOV     #010000,R5      ; set counter
       010000
003206 010311   2$:     MOV     R3,(R1)         ; output dac A
003210 010412           MOV     R4,(R2)         ; output dac B
003212 005305           DEC     R5              ; decrement counter
003214 001403           BEQ     3$              ; start down ramp
003216 005304           DEC     R4              ; decrement ramp B
003220 005203           INC     R3              ; bump ramp A
003222 000771           BR      2$              ; repeat
                ;
003224 012705   3$:     MOV     #010000,R5      ; initialize counter
       010000
003230 010311   4$:     MOV     R3,(R1)         ; output dac A
003232 010412           MOV     R4,(R2)         ; output dac B
003234 005305           DEC     R5              ; decrement counter
003236 001761           BEQ     1$              ; start over again
003240 005303           DEC     R3              ; decrement ramp A
003242 005204           INC     R4              ; bump ramp B
003244 000771           BR      4$              ; repeat
                ;
```

```
DT2781  TST11 MODULE   MACRO M11.  29-DEC-81 10:44  PAGE  1
SYMBOL TABLE

BASE  = 000542          DACTYP  000365R     002 TEST10  002276R     002
BIT0  = 000001          DEL     = 000177        TEST11  002374R     002
BIT1  = 000002          DELAY   = 000546        TEST12  002546R     002
BIT10 = 002000          DISPLY  002230R     002 TEST13  003040R     002
BIT11 = 004000          ERRCNT= 000522          TEST14  003160R     002
BIT12 = 010000          FF      = 000014        TEST15  003246R     002
BIT13 = 020000          GETCH   002022R     002 TEST16  003320R     002
BIT14 = 040000          INIT    000100R     002 TEST17  003376R     002
BIT15 = 100000          I2781   = 000100RG  002 TEST2   001024R     002
BIT2  = 000004          I2785   = 000100RG  002 TEST3   001206R     002
BIT3  = 000010          LF      = 000012        TEST4   001262R     002
BIT4  = 000020          NORPLY  000512R     002 TEST5   001370R     002
BIT5  = 000040          ODTACC= 000514          TEST6   001652R     002
BIT6  = 000100          PARAM   000422R     002 TEST7   002020R     002
BIT7  = 000200          PR7     = 000340        TIME    003024R     002
BIT8  = 000400          QUERY   000220R     002 TPB     000000R     002
BIT9  = 001000          RBUF    = 177562        T2781   = 000000RG  002
CHNL    000405R     002 RCSR    = 177560        T2785   = 000000RG  002
CODE  = 000020          REG     000566R     002 VECTOR= 000544
CR    = 000015          SPACE   = 000040        XBUF    = 177566
CTRLC = 000003          SPEED   000342R     002 XCSR    = 177564
CTRLI = 000011          SWR     = 000540        . ARG1= 000027
DAC     002754R     002 TEST1   000726R     002 . ARG2= 000000

  ABS   000000      000
          00        001
DT2781  003530      002
ERRORS DETECTED:  0

VIRTUAL MEMORY USED:  2956 WORDS  ( 12 PAGES)
DYNAMIC MEMORY:  3878 WORDS  ( 14 PAGES)
ELAPSED TIME:  00:01:00
DL1 2781,DL1:2781/NOSP=DL1:[1,2]TST11/ML,DL1 [100,21]2781.V01
```

```
                        .LIST   TTM
                        .ENABL  LC
                        .TITLE  SP0031  TS1-11 control module
                        .IDENT  /V01 02/
000000                  .PSECT  SP0031
                .NLIST  BIN
        ;
        ;
        ; Copyright (C) 1979, Data Translation Incorporated  All
        ; rights reserved.No part of this program or publication
        ; may be reproduced without the prior written permission
        ; of  Data Translation Incorporated,  4 Strathmore Road,
        ; Natick, Mass. 01760.
        ;
        ;
        ; The information in this document is subject to change
        ; without  notice  and  should  not  be  construed as a
        ; commitment by Data Translation Incorporated
        ;
        ;
        ; Data Translation cannot assume any responsibility for
        ; the use of any portion of this software for other than
        ; its intended  diagnostic  purpose  in calibrating and
        ; testing  Data  Translation  manufactured  analog  and
        ; digital interface boards.
        ;
        ;
        ; Version 01-02
        ;
        ;
        ;
        ;
        ;
        ; This program module provides the interface between
        ; the testing routines for the DT2781 series of interface
        ; products and the Data Translation TS1-11 monitor
```

```
                        
000000  DIRECT::
000000  SP0031: .WORD   SP0031          ; linked address
000002          .WORD   SPCODE          ; pointer to string
000004          .BYTE   2               ; # of entries
000005          .BYTE   -1,-1,-1        ; reserved
                ;
                ; ENTRIES
                ;
                .GLOBL  I2781,T2781
000010          .ASCII  "2781"
000014          .WORD   I2781,T2781
                ;
                .GLOBL  I2785,T2785
000020          .ASCII  "2785"
000024          .WORD   I2785,T2785
                ;
                ;
000030  SPCODE: .ASCIZ  "SP-0031 V01-03 "
                .EVEN
                ;
                .END
```

```
SP0031  TSI-11 CONTROL MODULE   MACRO M1113  29-DEC-81 15:56  PAGE 2-1
SYMBOL TABLE

DIRECT  000000RG     002 SPCODE  000030R     002 T2781 = ****** G
I2781 = ****** G         SP0031  000000R     002 T2785 = ****** G
I2785 = ****** G

  ABS.  020000     000
        0000       001
SP0031  000050     002
ERRORS DETECTED:  0

VIRTUAL MEMORY USED:  140 WORDS  ( 1 PAGES)
DYNAMIC MEMORY:  2822 WORDS  ( 10 PAGES)
ELAPSED TIME:  00.00:03
DL1.SP0031,DL1:SP0031/NOSP=DL1:SP0031.V01
```

```
RT-11 LINK  V06.01       Load Map         Fri 04-Dec-81 00:00:00
SP0031.LDA       Title:  SP0031  Ident:  V01.02

Section  Addr    Size     Global  Value   Global  Value   Global  Value

 . ABS.  000000 001000    (RW,I,GBL,ABS,OVR)
 SP0031  001000 000050    (RW,I,LCL,REL,CON)
                         DIRECT  001000
 DT2781  001050 003530    (RW,I,LCL,REL,CON)
                         T2781   001050  T2785   001050  I2781   001150
                         I2785   001150
 TST11   004600 006474    (RW,I,LCL,REL,CON)
                         START   004600

Transfer address = 004600, High limit = 013272 = 2909.  words
```

APPENDIX B

CIRCUIT SCHEMATICS

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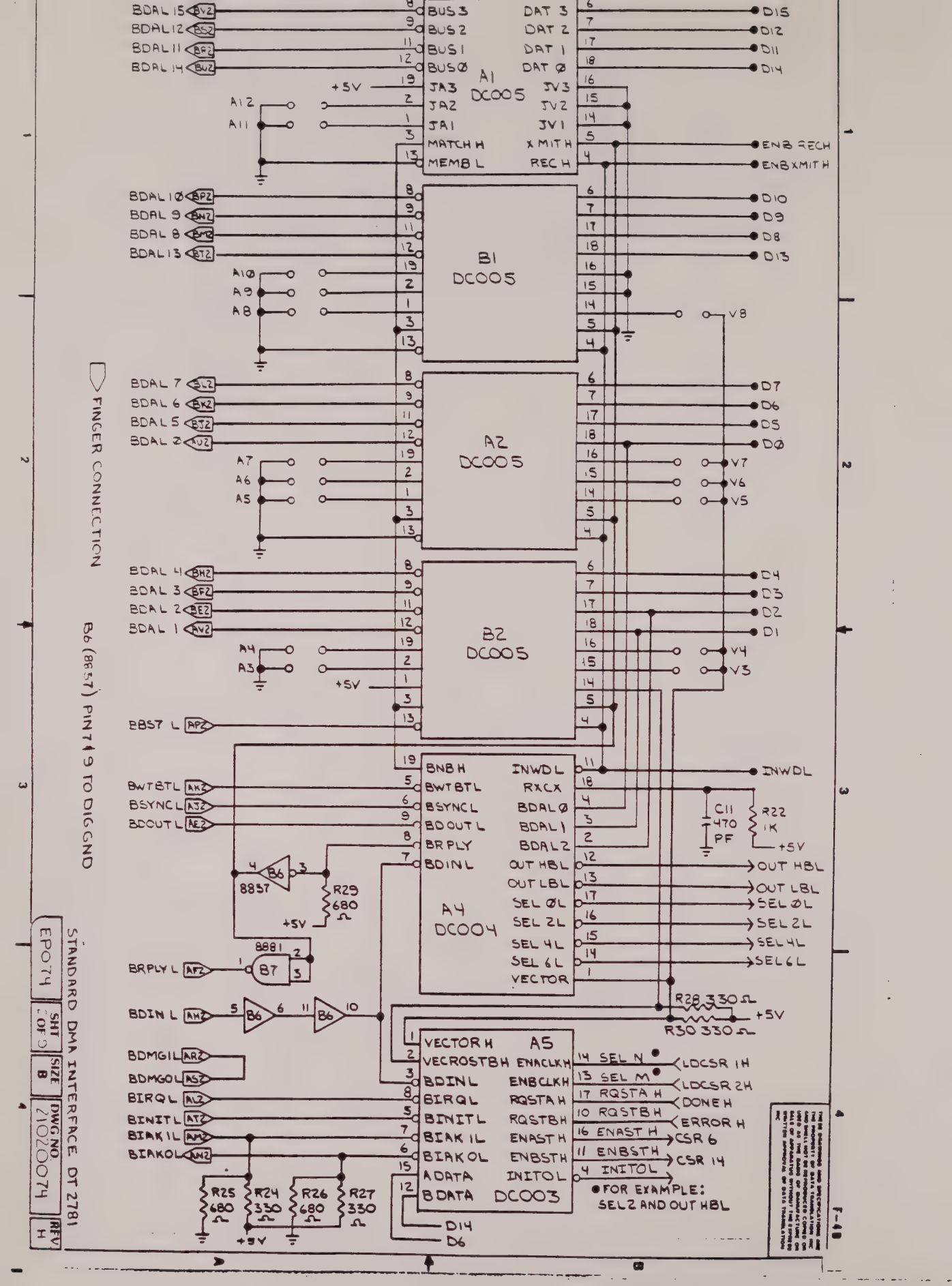
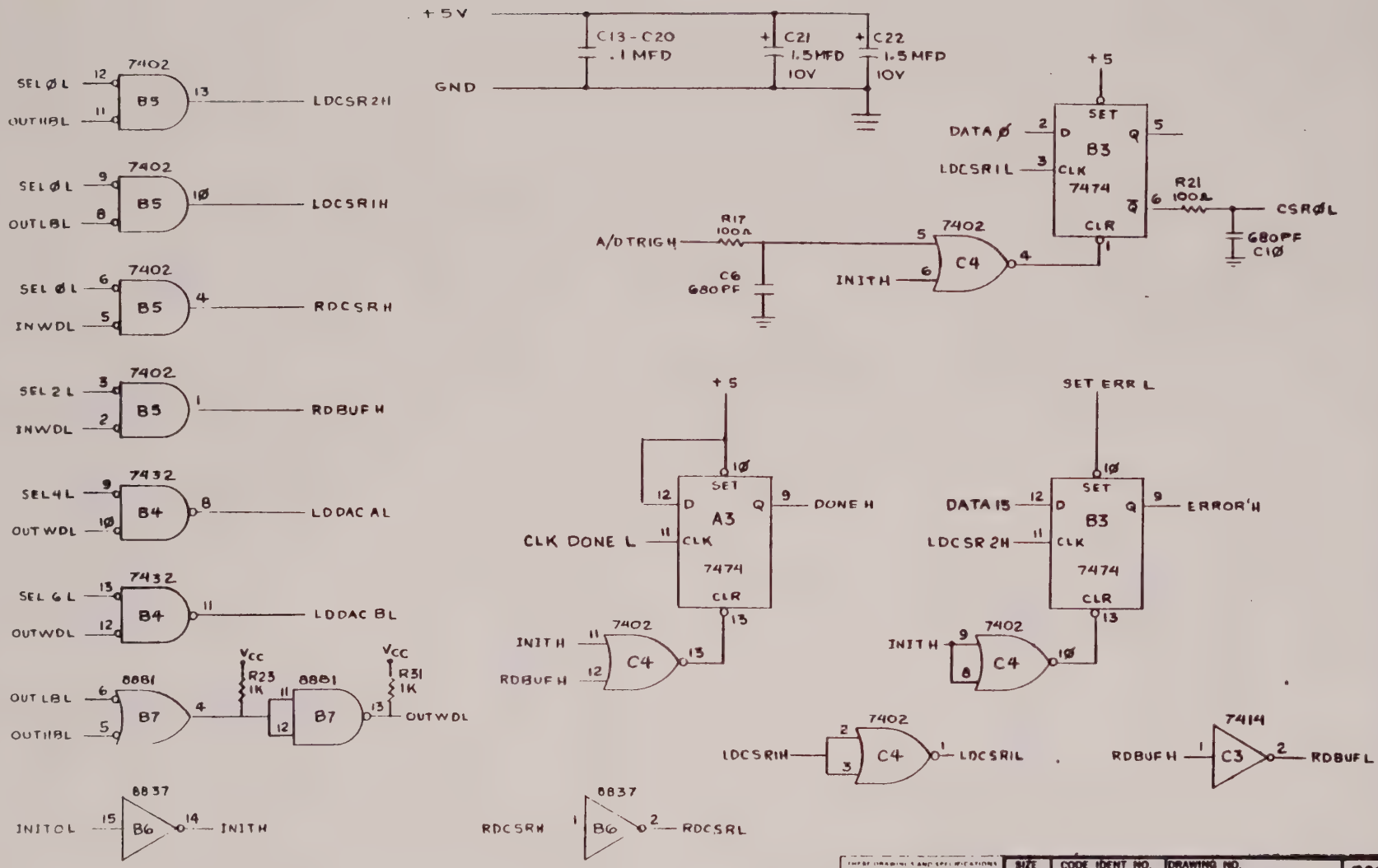
REVISION	ECO NO.	DATE	DWN	ENG
H	517	4-27 82	K.Y.C.	
G	479	3-26-82	K.Y.C.	
F	429	12-30-81	K.Y.C.	
E	349	5-4-81	K.Y.C.	
D-2	297-R	12-23-80	K.Y.C.	
D-1	278-R	9-10-80		
D	260	6-20-80	K.Y.C.	
C	203	10-16-79	K.Y.C.	
B	184	8-6-79	K.Y.C.	

DATA TRANSLATION INC

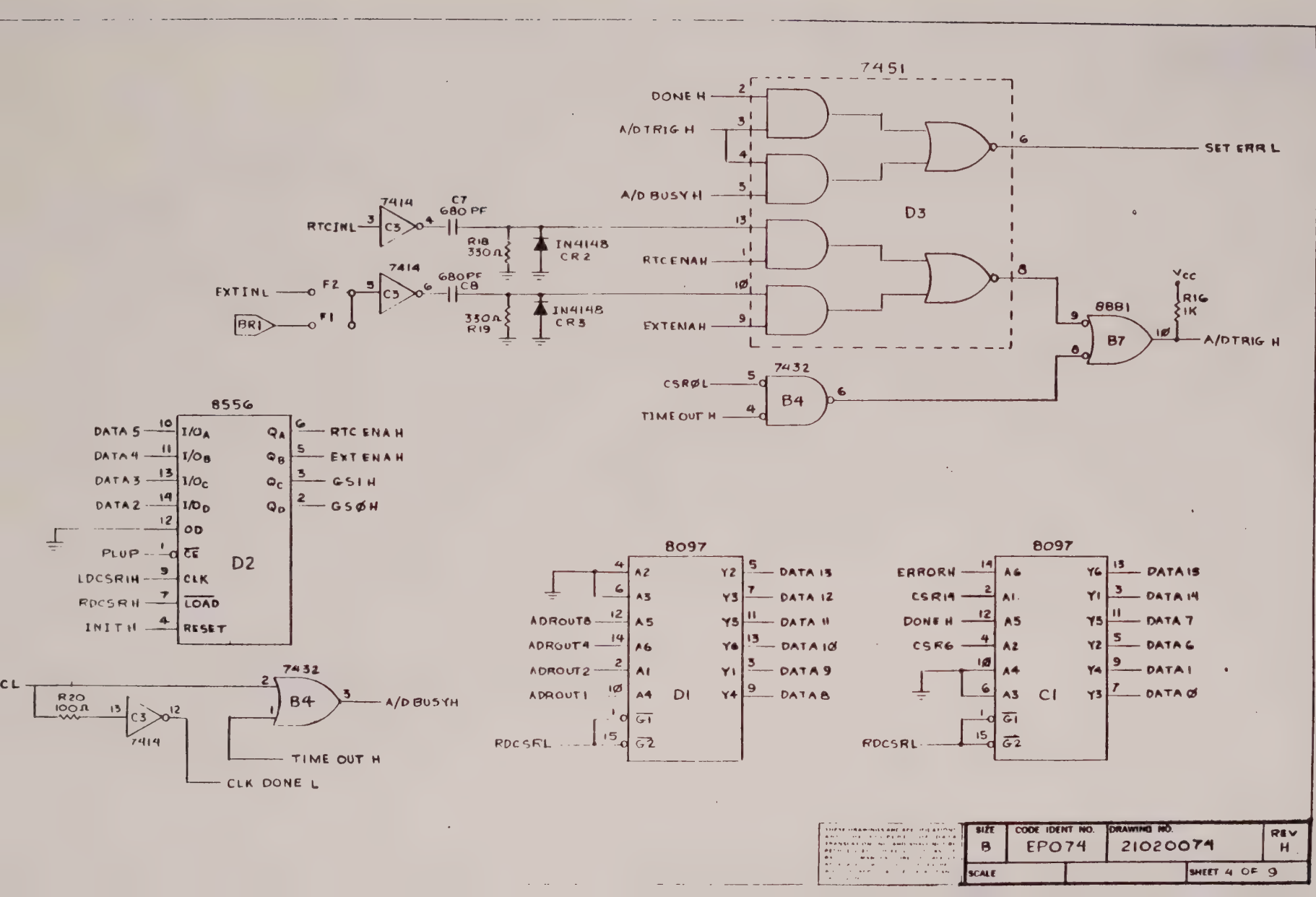
DRAWN: K.Y.C.	DATE: 6-19-79	TITLE: SCHEMATIC DT 2781
CHECKED: K.E.D.	DATE: 6-19-79	
ENG:	DATE: 9-16-79	

EP074	SHT. 1 OF 9	SIZE B	DWG NO. 21020074	REV. H


BDAL 15
BDAL 12
BDAL 11
BDAL 14
BUS 3
BUS 2
BUS 1
BUS Ø
DAT 3
DAT 2
DAT 1
DAT Ø
D15
D12
D11
D14
A1
DC005
+5V
A12
A11
JA3
JA2
JA1
JV3
JV2
JV1
MATCH H
MEMB L
XMIT H
REC H
ENB RECH
ENB XMIT H
BDAL 10
BDAL 9
BDAL 8
BDAL 13
B1
DC005
A10
A9
A8
D10
D9
D8
D13
V8
BDAL 7
BDAL 6
BDAL 5
BDAL Ø
A2
DC005
A7
A6
A5
D7
D6
D5
DØ
V7
V6
V5
BDAL 4
BDAL 3
BDAL 2
BDAL 1
B2
DC005
A4
A3
+5V
D4
D3
D2
D1
V4
V3
BBS7 L
BNB H
BWTBTL
BSYNC L
BDOUT L
BRPLY
BDIN L
INWDL
RXCX
BDAL Ø
BDAL 1
BDAL 2
OUT HBL
OUT LBL
SEL ØL
SEL 2L
SEL 4L
SEL 6L
VECTOR
A4
DC004
INWDL
C11
470
PF
R22
1K
+5V
OUT HBL
OUT LBL
SEL ØL
SEL 2L
SEL 4L
SEL 6L
B6
8837
R29
680
+5V
B7
8881
BRPLY L
BDIN L
B6
B6
R28 330
R30 330
+5V
BDMGI L
BDMGO L
BIRQ L
BINIT L
BIAKI L
BIAKO L
VECTOR H
VECROSTBH
BDIN L
BIRQ L
BINIT L
BIAKI L
BIAKO L
ADATA
BDATA
DC003
A5
ENACLKH
ENBCLKH
RQSTA H
RQSTB H
ENAST H
ENBST H
INITO L
SEL N
SEL M
RQSTA H
RQSTB H
ENAST H
ENBST H
INITO L
LDCSR 1H
LDCSR 2H
DONE H
ERROR H
CSR 6
CSR 14
●FOR EXAMPLE:
SEL2 AND OUT HBL
R25
680
R24
330
R26
680
R27
330
+5V
D14
D6
FINGER CONNECTION
B6 (8837) PIN 7 TO DIGGND
STANDARD DMA INTERFACE DT 2781
EPO 74
SHT 2 OF 9
SIZE B
DWG NO 2020074
REV H
F-48



SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	H
SCALE		SHEET 3 OF 9	



SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	H
SCALE		SHEET 4 OF 9	

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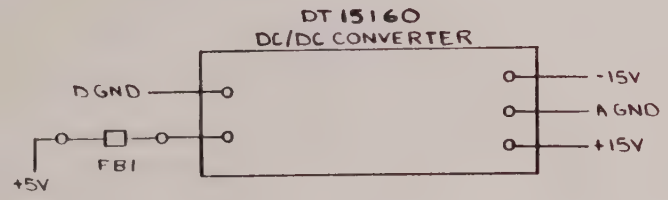

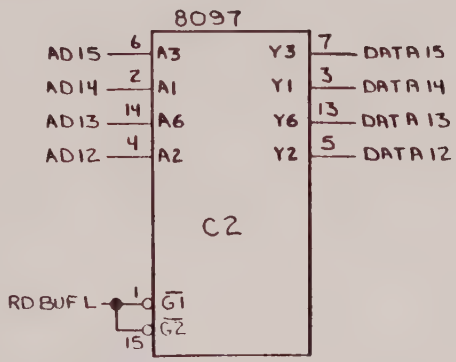

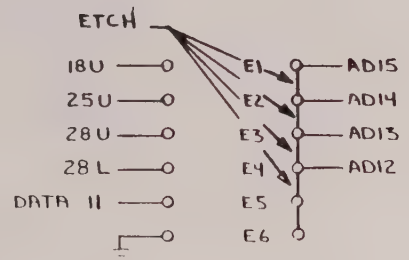

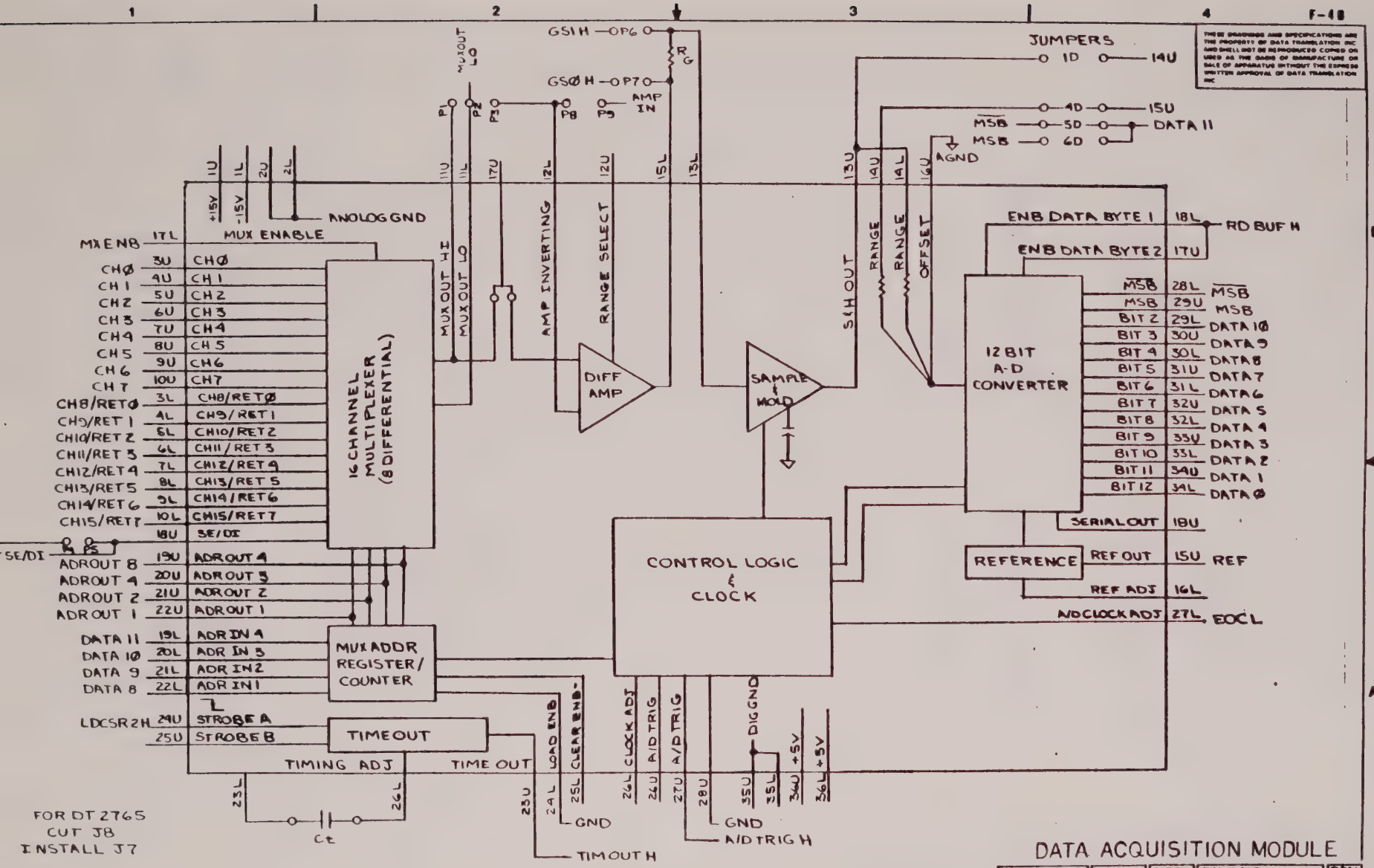

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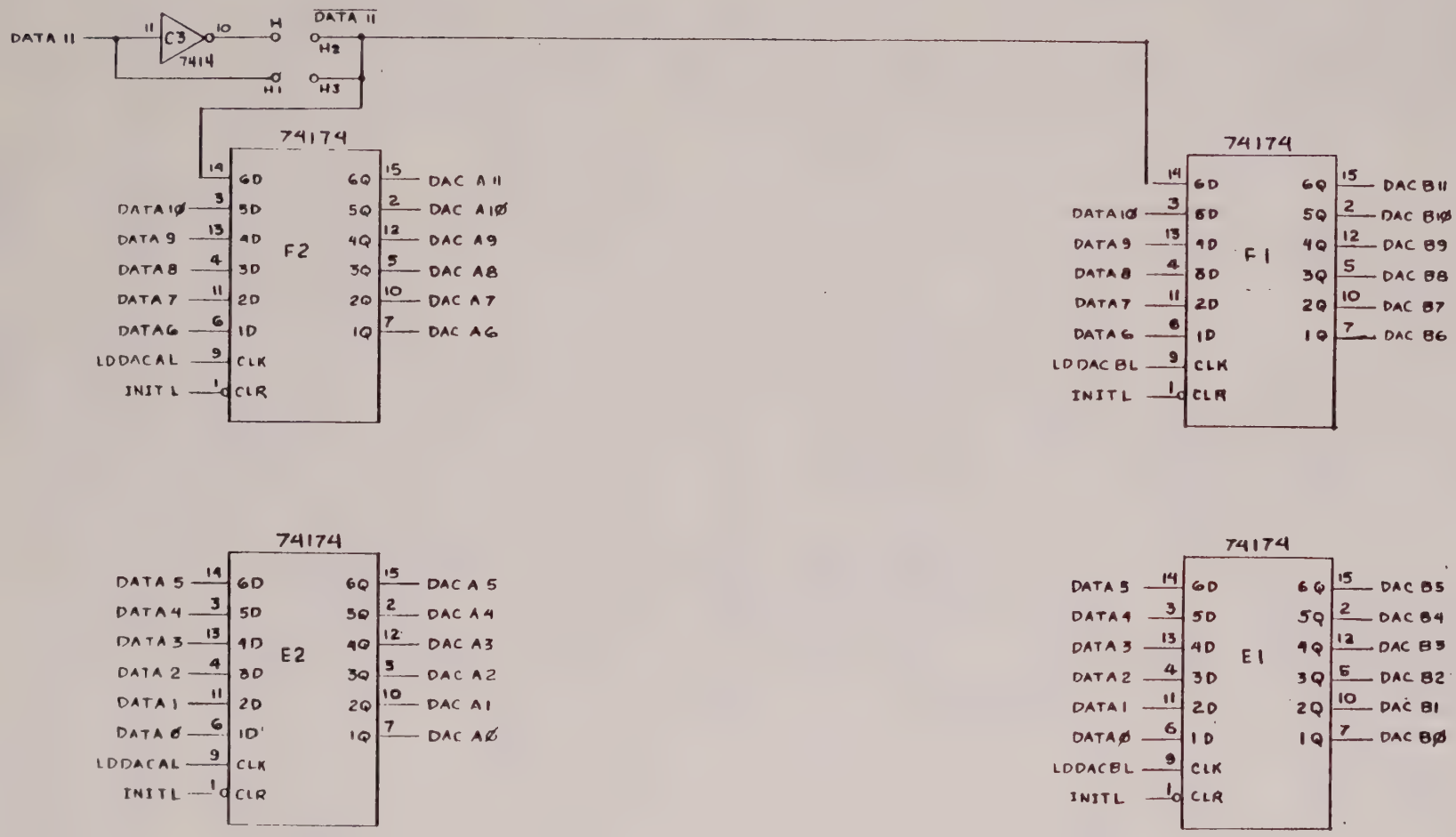
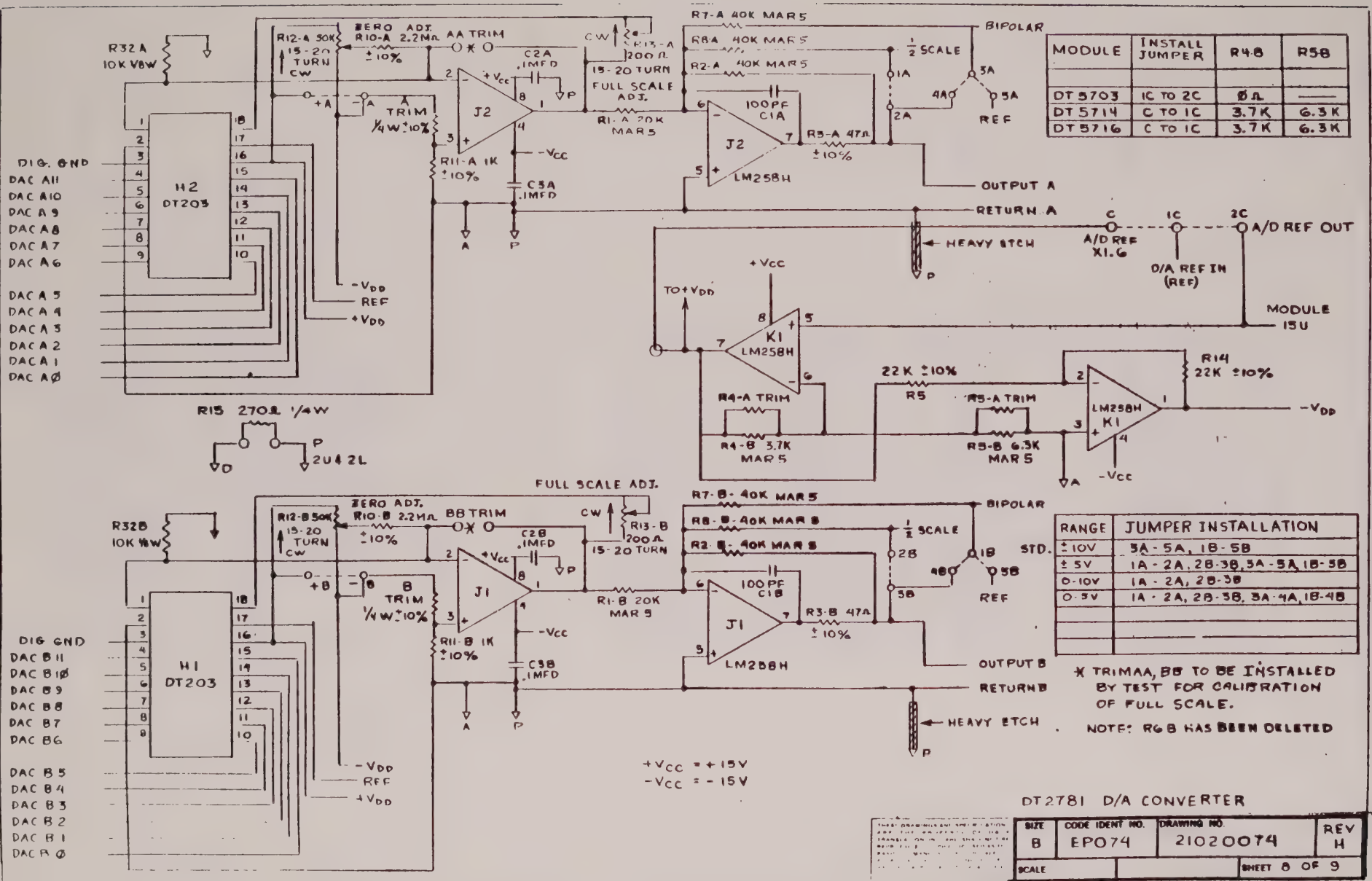
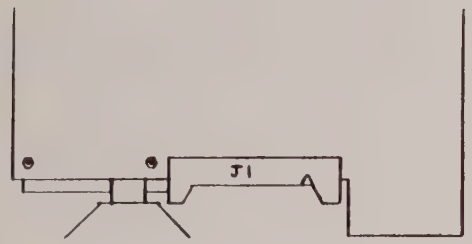
DATA ACQUISITION MODULE

EP074	SHT 6 OF 9	SIZE B	DWG NO 21020074	REV H



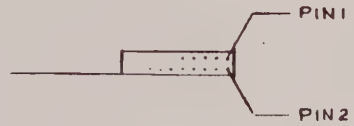
SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	H
SCALE		SHEET 7 OF 9	

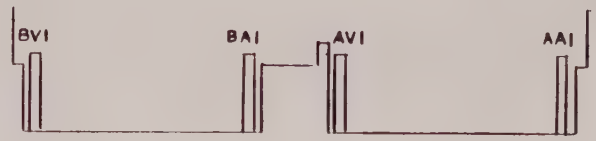

R32A 10K V8W
R12-A 30K 15-20 TURN CW
ZERO ADJ. R10-A 2.2MΩ ±10%
AA TRIM
C2A .1MFD
R13-A 200Ω 15-20 TURN
FULL SCALE ADJ.
R1-A 20K MAR 5
R11-A 1K ±10%
C3A .1MFD
+A
A TRIM 1/4W ±10%
J2
LM258H
+Vcc
-Vcc
R7-A 40K MAR 5
R8-A 40K MAR 5
R2-A 40K MAR 5
100PF C1A
R3-A 47Ω ±10%
BIPOLAR
1/2 SCALE
1A
2A
3A
4A
5A
REF
OUTPUT A
RETURN A
HEAVY ETCH
C
A/D REF X1.6
1C
D/A REF IN (REF)
2C
A/D REF OUT
MODULE 15U
H2 DT203
DIG. GND
DAC A11
DAC A10
DAC A9
DAC A8
DAC A7
DAC A6
DAC A5
DAC A4
DAC A3
DAC A2
DAC A1
DAC AØ
-VDD REF
+VDD
R15 270Ω 1/4W
D
P
2U & 2L
TO +VDD
K1 LM258H
22K ±10%
R5
R4-A TRIM
R4-B 3.7K MAR 5
R5-A TRIM
R5-B 6.3K MAR 5
R14 22K ±10%
-VDD
-Vcc
MODULE | INSTALL JUMPER | R4-B | R5-B
DT 5703 | IC TO 2C | ØΩ | —
DT 5714 | C TO 1C | 3.7K | 6.3K
DT 5716 | C TO 1C | 3.7K | 6.3K
FULL SCALE ADJ.
R32B 10K V8W
R12-B 30K 15-20 TURN CW
ZERO ADJ. R10-B 2.2MΩ ±10%
BB TRIM
C2B .1MFD
R13-B 200Ω 15-20 TURN
R1-B 20K MAR 5
R11-B 1K ±10%
C3B .1MFD
+B
B TRIM 1/4W ±10%
J1
LM258H
R7-B 40K MAR 5
R8-B 40K MAR 5
R2-B 40K MAR 5
100PF C1B
R3-B 47Ω ±10%
BIPOLAR
1/2 SCALE
1B
2B
3B
4B
5B
REF
STD.
OUTPUT B
RETURN B
HEAVY ETCH
H1 DT203
DIG GND
DAC B11
DAC B10
DAC B9
DAC B8
DAC B7
DAC B6
DAC B5
DAC B4
DAC B3
DAC B2
DAC B1
DAC BØ
-VDD REF
+VDD
+Vcc = +15V
-Vcc = -15V
RANGE | JUMPER INSTALLATION
±10V | 3A-5A, 1B-5B
±5V | 1A-2A, 2B-3B, 3A-5A, 1B-5B
0-10V | 1A-2A, 2B-3B
0-5V | 1A-2A, 2B-3B, 3A-4A, 1B-4B
* TRIMAA, BB TO BE INSTALLED BY TEST FOR CALIBRATION OF FULL SCALE.
NOTE: R6B HAS BEEN DELETED
DT2781 D/A CONVERTER
SIZE B
CODE IDENT NO. EP074
DRAWING NO. 21020074
REV H
SCALE
SHEET 8 OF 9



J1 CONNECTOR			
PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	CH Ø	2	CH 8 / RET Ø
3	CH 1	4	CH 9 / RET 1
5	CH 2	6	CH 10 / RET 2
7	CH 3	8	CH 11 / RET 3
9	CH 4	10	CH 12 / RET 4
11	CH 5	12	CH 13 / RET 5
13	CH 6	14	CH 14 / RET 6
15	CH 7	16	CH 15 / RET 7
17	A GND	18	AMP IN
19	EXT TRIG L	20	D GND
21	RTCINL	22	D GND
23	DAC A RET	24	DAC A OUT
25	DAC B RET	26	DAC B OUT

RTCINL ON WIRE POST





BOTTOM EDGE CONNECTOR							
COMPONENT SIDE		SOLDER SIDE		COMPONENT SIDE		SOLDER SIDE	
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
BA1		BA2	+ 5V	AA1		AA2	+ 5V
BB1		BB2		AB1		AB2	
BC1		BC2	D GND	AC1		AC2	D GND
BD1		BD2		AD1		AD2	
BE1		BE2	BDAL 2L	AE1		AE2	BD OUT L
BF1		BF2	BDAL 3L	AF1		AF2	BRPLY L
BH1		BH2	BDAL 4L	AH1		AH2	BDIN L
BJ1	D GND	BJ2	BDAL 5L	AJ1	D GND	AJ2	BSYNC L
BK1		BK2	BDAL 6L	AK1		AK2	BWT BTL
BL1		BL2	BDAL 7L	AL1		AL2	BIRQ L
BM1	D GND	BM2	BDAL 8L	AM1	D GND	AM2	BIAK IL
BN1		BN2	BDAL 9L	AN1		AN2	BIAK OL
BP1		BP2	BDAL 10L	AP1		AP2	BBS 7L
BR1	BEVNT	BR2	BDAL 11L	AR1		AR2	BDMG IL
BS1		BS2	BDAL 12L	AS1		AS2	BDMG OL
BT1	D GND	BT2	BDAL 13L	AT1	D GND	AT2	BINITL
BU1		BU2	BDAL 14L	AU1		AU2	BDALOL
BV1	+ 5V	BV2	BDAL 15L	AV1		AV2	BDALIL

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	EP074	21020074	H
SCALE		SHEET 9 OF 9	

INTRODUCTON TO "INTERFACE BOARD A/D CALIBRATION PROCEDURE"

The following document provides detailed information on calibrating the following Data Translation A/D converters:

1. DT5701;
2. DT5702;
3. DT5703;
4. DT5710;
5. DT5720;
6. DT5740;
7. DT5722;
8. DT6812;
9. DT2009;
10. DT5712;
11. DT5711;
12. DT5714;
13. DT5716;
14. DT5704.

This calibration procedure is divided into discussions of the following: single-ended (section 5.000) versus differential mode (section 6.000); calibration (section 7.000) for unipolar and bipolar ranges; applications (section 8.000), which indicates a number of recommended procedures for improving A/D performance; and troubleshooting (section 9.000). Coding charts and a list of recommended test equipment are also given.

INTERFACE BOARD A/D CALIBRATION PROCEDURE

1.000 INTRODUCTION

1.010 This procedure will cover the calibration of a typical A/D converter, unipolar or bipolar, 12 to 16 bit, using a microcomputer.

1.020 In addition it will provide the hook-up diagrams for single ended and differential operation along with recommended ground connections.

2.000 ASSUMPTIONS

2.010 Calibration will be done on channel 0 with all other channels returned to analog common.

2.020 The input cable is less than 3 meters long.

2.030 Software is available to provide continuous readings of channel 0 and display them on a CRT.

3.000 EQUIPMENT REQUIRED

3.010 Precision voltage source, Electronic Development Corporation model 501J, or equivalent.

3.020 Miscellaneous cables and connectors.

4.000 PRECAUTIONS

4.010 Switch the computer power off when installing or removing the interface board.

4.020 Switch the reference signal (which connects to the analog multiplexer) on only when the board is under power. This will prevent damage to interface boards without multiplexer input protection. A 510 ohm resistor may be installed in series with the input to provide multiplexer protection to ±10 volts with the power off.

5.000 SINGLE ENDED OPERATION (SE)

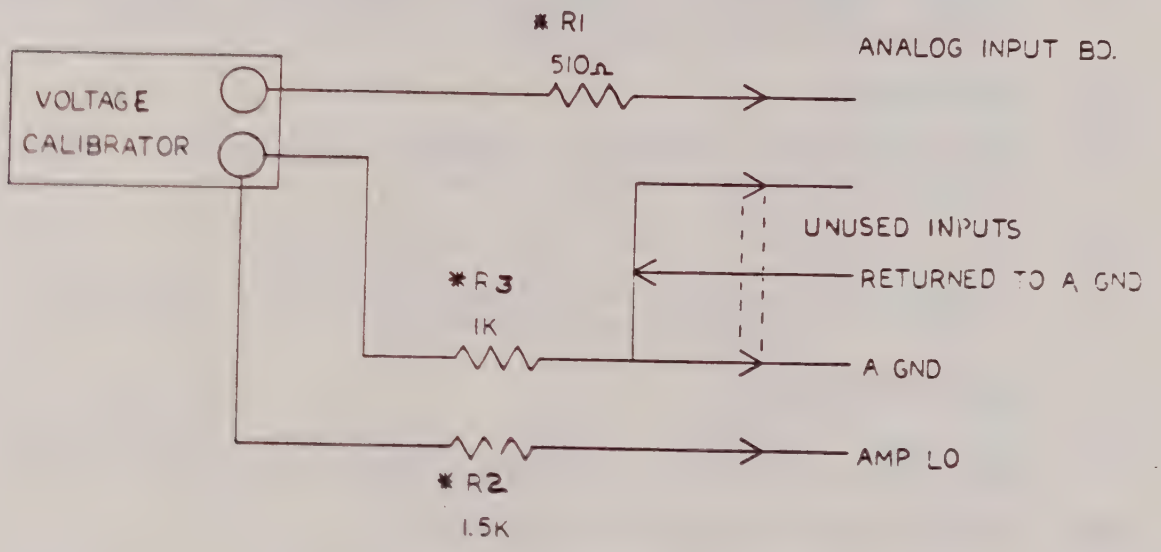
5.010 In the SE mode, all the analog inputs are referenced to a single ground potential.

5.020 If the input has provision for pseudo-differential operation the amplifier lo can be used as a remote ground sense connection to reject a single common mode voltage on all inputs.

5.021 For proper operation the amplifier lo input must be connected to the signal common as close to the signal as possible.

5.022 Note that the input can be balanced by placing the same impedance in series with the amplifier lo input as there is in the signal paths. (Typically, 1 kilohm for the multiplexer plus 1 kilohm for signal source impedances or 2 kilohms total.) Additionally the 2 kilohm resistor will provide current limiting for over voltage conditions.

5.030 HOOK-UP SE



* R1, R2 + R3 OPTIONAL AND MAY BE REPLACED WITH A DIRECT CONNECTION

5.031 R1 is used for input protection.

5.032 R2 is used to balance the amplifier input and represents 1 kilohm for the multiplexer plus 500 ohms for the input protecton resistor R1.

5.033 R3 isolates the calibrator lo signal from the analog ground.

6.000 DIFFERENTIAL INPUT OPERATION (DI)

6.010 In the differential mode of operation each input has a hi (ch0) and a lo (ch0 Ret) connection. The measurement taken is the difference between the two inputs, thereby rejecting any noise common to both inputs.

6.020 With non-isolated systems, care must be taken to insure that the inputs are referenced to analog common.

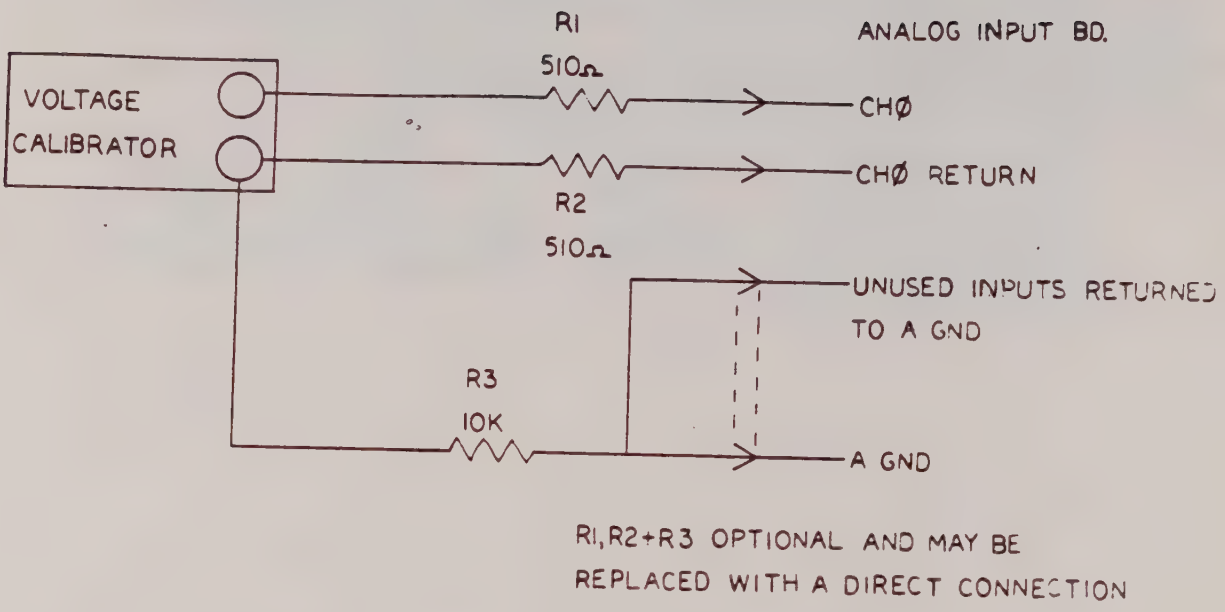
6.021 If the signal to be measured is isolated, a return path for the bias current must be provided back to analog

common. This may be done by connecting a 1 kilohm to 100 kilohm resistor from the signal lo to analog common.

6.022 If all analog inputs are referenced to a single analog common, only one resistor will be required.

6.023 A direct connection could be made; however, this could cause large ground currents to flow if the computer ground potential is several volts different from the input signal ground potential. Even if the signal inputs are isolated from earth ground AC currents could flow due to stray capacitance.

6.030 HOOK-UP DI



6.031 R1 and R2 are used for input protection.

6.032 R3 is used to reference the inputs to analog common. Otherwise, they may drift due to bias currents out of the common mode voltage range.

7.000 CALIBRATION

7.001 Allow one hour for the entire system to warm up and stabilize before calibration.

7.010 With software programmable gains the calibration must be done at the gain of 1 first.

7.020 With resistor programmable gain, the calibration is done after the resistor to determine the gain has been installed.

7.030 With jumper selectable gain, the calibration will be done on the selected range.

7.040 When adjusting the potentiometers, center the code on the proper value by noting where the adjacent codes are. That is, mechanically center the pot between the position that yields the desired value plus 1 LSB and the desired value minus 1 LSB.

7.041 A second calibration must be done to eliminate interaction between the adjustments.

7.042 When calibrating an isolated system with PGL gain, the high level (gain of 1) must be done on one channel and

the low level (gain greater than 10) done on another. Otherwise, up to 1 hour could be required to discharge the capacitor when the gain is switched from 1 to 500.

7.050 At the present time, all Data Translation 14-bit converters have all 16 bits brought out and must be calibrated as 16-bit converter.

7.060 On a ±10 volt input, the range is 20V. (Range equals the upper input voltage minus the lower input voltage. For ±10V, that is +10V - (-10V) = 20V range.)

7.070 LSB TABLE

INPUT RANGE*	1 LSB SIGNAL FOR: 12 BITS	14 BITS	16 BITS
20V (+/-10V)	4.88 mV	1.221 mV	305.2 uV
10V (+/-5V)	2.44 mV	610.4 uV	152.6 uV
5V (+/-2.5V)	1.22 mV	305.2 uV	76.29 uV
1.25V (+/-.625V)	305 uV	76.29 uV	19.07 uV
.625V (+/-.3125V)	152 uV	38.15 uV	9.537 uV
.100V (+/-50 mV)	24.4 uV	6.104 uV	1.526 uV
20 mV (+/-10 mV)	4.88 uV	1.221 uV	305.2 nV
10 mV (+/-5 mV)	2.44 uV	610.4 nV	152.6 nV
4 mV (1-5V)	976 uV	244.1 uV	61.04 uV
16 Ma (4-20mA)	3.91 uA	976.6 nA	244.1 nA

7.080 +FULL SCALE -2 LSB VOLTAGE

INPUT RANGE*	12 BIT A/D	14/16 BIT A/D
20V (+/-10V)	9.9902V	9.99939V
10V (0 to +10V)	9.9951V	9.99969V
5V (0 to +5V)	4.9976V	4.99985V
2.5V (0 to +2.5V)	2.4988V	2.49992V
1.25V (0 to +1.25V)	1.2494V	1.24996V
.635V (0 to +.625V)	.62469V	.624981V
.100V (0 to +.100V)	99.951 mV	99.9969 mV
20 mV (0 to +20 mV)	19.990 mV	19.9994 mV
10 mV (0 to +10 mV)	9.9951 mV	9.99969 mV
4V (1-5V)	4.9980V	4.99988 mV
16 mA (4-20mA)	19.992 mA	19.9995 mA

7.090 FULL SCALE -2 LSB OUTPUT CODE STRAIGHT BINARY CODE

BITS	BINARY	OCTAL	HEX
12	111 111 111 110	007776	OFFE
14/16	1 111 111 111 111 110	177776	FFFE

7.091 2'S COMPLEMENT CODE

BITS	BINARY	OCTAL	HEX
12	011 111 111 110	003776	07FE
14/16	0 111 111 111 111 110	077776	7FFE

*See 7.060 for a definition of range

7.100 UNIPOLAR ZERO

7.110 Input 1 LSB of signal (note table 7.070) and adjust the offset or zero adjust potentiometer for 1 count on the digital output.

7.120 On the higher gain ranges, especially at 14 or 16 bits, the input can be increased to 10 LSB's to center up the outputs around 10 LSB's due to the noise level.

7.200 UNIPOLAR FULL SCALE

7.210 Input plus full scale minus 2 LSB's and adjust the range or full scale potentiometer for the proper code per 7.080.

7.220 On the higher gain ranges, especially at 14 or 16 bits, the input can be reduced 10 LSB's to center up the outputs around full scale minus 10 LSB's.

7.300 PGL AND PGH ZERO

7.310 To calibrate the zero on software programmable gain models (PGL and PGH), first calibrate the zero and full scale at a gain of 1.

7.320 Switch the gain to maximum and apply an input of 1 LSB of the range. For example, at a gain of 8, the full scale range would be 1.25 volts. Thus the input would be 305uV for a 12-bit converter.

7.330 Adjust the amplifier or auxiliary offset for 1 digital count. (Note 7.120)

7.400 BIPOLAR ZERO (2'S COMPLEMENT CODE)

There are two different zero adjustment procedures on bipolar units. Care must be taken to insure that the correct procedure is used. Otherwise, there will be excessive interactions between the zero and full scale adjustments.

7.402 The difference between the two adjustments is that one type is adjusted with zero volts at the input where the other is adjusted with minus full scale plus 1 LSB at the input.

7.403 The following is a list of modules that may be installed on an interface board that requires zero volts at the input for zero calibration:

DT5701	DT5740
DT5702	DT5722
DT5703	DT6812
DT5710	DT2009
DT5720	

7.404 The following is a list of modules that may be installed on an interface board that requires minus full scale plus 1 LSB at the input for zero calibration:

DT5711	DT5716
DT5712	DT5704
DT5714	

7.410 ZERO CALIBRATION (NOTE 7.4030)

7.411 Input zero volts and adjust the zero potentiometer for all zeros output.

7.420 ZERO CALIBRATION (NOTE 7.404)

7.421 Input minus full scale plus 1 LSB voltage and adjust the zero potentiometer for the correct output code per the table 7.440.

7.430 Minus full scale + 1 LSB output code.

7.431 2'S COMPLEMENT CODE (-FS + 1 LSB) (SIGN EXTENDED)

BITS	BINARY	OCTAL	HEX
12	1 111 100 000 000 001	174001	F801
14/16	1 000 000 000 000 001	100001	8001

7.440 MINUS FULL SCALE + 1 LSB VOLTAGE

INPUT RANGE	12 BIT A/D	14/16 BIT A/D
20V (+/-10V)	-9.9951V	-9.99969V
10V (+/-5V)	-4.9976V	-4.99985V
5V (+/-2.5V)	-2.4988V	-2.49992V
2.5V (+/-1.25V)	-1.2494V	-1.24996V
1.25V (+/-.625V)	-.62469V	-.624981V
.625V (+/-.312V)	-.31235V	-.312490V
.2V (+/-.1V)	-99.950 mV	-99.9969 mV
.1V (+/-.05V)	-49.976 mV	-49.9985 mV
40 mV (+/-20 mV)	-19.990 mV	-19.9994 mV
20 mV (+/-10 mV)	-9.9951 mV	-9.99969 mV
10 mV (+/-5 mV)	-4.9976 mV	-4.99985 mV

7.500 BIPOLAR FULL SCALE

7.510 Input plus full scale minus 2 LSB's and adjust the range on full scale potentiometer for the proper code per 7.080.

7.511 On the higher gain ranges, especially at 14 or 16 bits, the voltage input can be reduced 10 LSB's to center the output around full scale minus 10 LSB's.

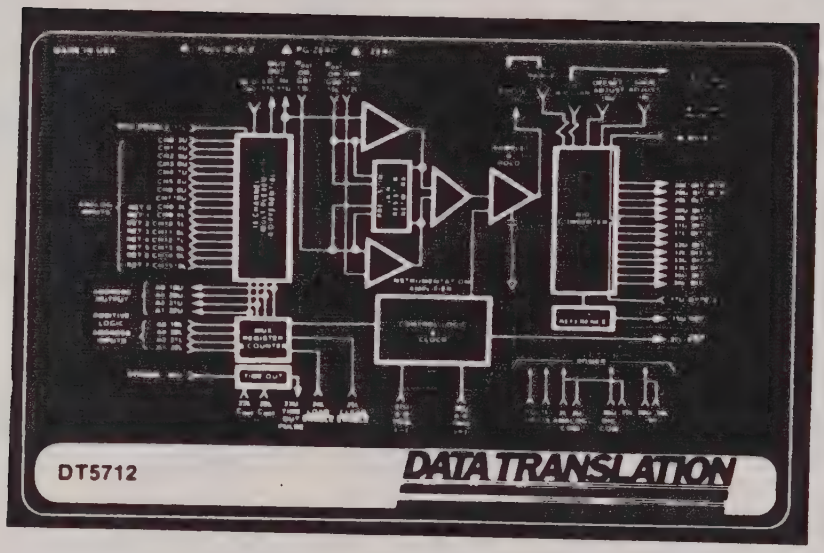
7.600 PGL AND PGH ZERO

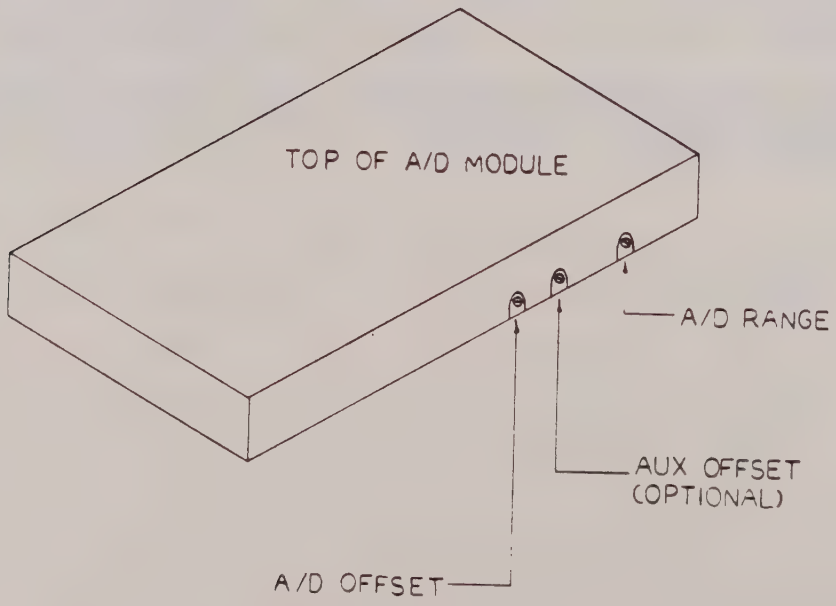
7.610 To calibrate the zero on software programmable gain models (PGL, PGH), first calibrate the zero and full scale at a gain of 1.

7.620 At a gain of 1, apply 0 volts at the input and note the digital output code. It must be all zeros ±1 LSB.

7.630 Set the software programmable gain to maximum and adjust the PG zero or auxiliary zero for all zeros on the digital output.

7.800 POTENTIOMETER LOCATIONS





8.000 APPLICATIONS

8.010 Noise is the major problem with A/D converters. In addition to the accuracy specifications, there is an added noise specification of .2 LSB rms at a gain of 1. In addition, the input amplifier has a noise specification that is multiplied by gain. (3 uV for 12 bits and 1 uV rms for 16 bits.)

8.011 To determine the peak to peak spread of the noise to the 3-sigma points (99.7%), the rms value is multiplied by 6.

8.012 COUNT SPREAD DUE TO NOISE (±10V A/D RANGE)

GAIN	12 BIT A/D	16 BIT A/D
AV = 1	1.2	1.2
8	1.2	1.2
100	1.2	2.3
500	2.2	9.9
1,000	3.9	19.7

8.020 Single ended operations for gains up to 10, A/D conversion rates to 40kHz with a low single source impedance and cable lengths less than 3 meters are usually fine.

8.021 Other than the previous conditions in 8.020, differential inputs should be used.

8.022 All cables must be routed away from switching power supplies and digital signals.

8.023 In high noise environments, the inputs must be differential with shielded twisted pairs for the signal.

8.024 The shield should only be connected at one end.

8.025 Unused inputs should be returned to analog common.

8.026 RC filters can be added at the inputs to remove high frequency noise pick-up.

8.027 Digital averaging of the data can be done simply by adding 16 12-bit A/D conversions and then shifting right 4 times (divided by 16). This is especially useful to minimize the rms noise in high gain applications.

8.100 Input settling time can be a problem if the input cable is over 3 meters in length or the source impedance over 1 kilohm.

8.110 With the following modules, a capacitor can be installed on the board (CT) to allow additional settling time. Note that source impedances greater than 10 kilohms are not recommended due to input impedance errors and bias current errors.

DT5702	DT5722
DT5712	DT5704
DT5714	
DT5716	

8.111 A typical DT5712 hook-up with 3 meters of cable and a source impedance of 10 kilohms requires a 1 nF capcitor in the CT position. This reduces the maximum throughput to approximately 20kHz.

8.200 GROUNDING

8.210 DIFFERENTIAL INPUTS

When the differential input scheme is utilized, there are two switches per channel. Thus the number of channels is cut in half. The benefits are that common mode voltages, i.e., voltages appearing on both sides of the source simultaneously can be rejected by the differential input instrumentation amplifier. This Common Mode Rejection (CMR) results in a much quieter system. The amount of CMR depends on how well balanced the impedances are on the instrumentation amplifier inputs. (Typical spec. of 80dB at @ 60Hz with 1 kilohm unbalanced.)

8.211 One problem that the user must realize is that even though you have a differential input, the inputs must be referenced back to the analog common of the system. This is because the signal plus common mode voltage range of the input is ±11 volts and if the input is not referenced back to analog common, leakage currents on the input will drive the inputs out of the common mode voltage range thereby saturating the amplifier.

8.212 This ground reference need not be a hard connection but some impedance from 1 kilohm to 100 kilohms.

8.213 It is recommended that this connection be made with a 1 kilohm to 100 kilohm impedance rather than a direct connection to minimize potential ground current through the analog system. For example, the computer analog ground system eventually would be connected back to earthground at a different location, several volts of ground potential between the two could result. If the connections are connected directly, several amps of current could flow through the analog path creating noisy data. If the connection is made through a 1 kilohm impedance, one volt ground difference will only cause one milliamp of current through the analog path thereby creating the minimum disturbance to the analog measuring system. Note hook-up at 6.030, (R3).

8.214 If all the analog inputs have a common connection, the resistor need only be installed once between the two commons.

8.220 SINGLE ENDED INPUTS

8.221 With single ended inputs it is recommended that the inputs be isolated from earthground.

8.222 All the signal commons then would be connected separately to analog common of the board.

8.230 PSEUDO-DIFFERENTIAL

8.231 This mode of operation allows one common mode voltage for all inputs.

8.232 The amplifier low input is used as a remote ground sense wire.

8.233 For example, a metal panel could be used with BNC connectors mounted on it with a common ground. A 1 kilohm resistor could be connected between the panel and analog common to prevent the ground from floating out of the common mode voltage range due to bias currents if the ground is floating. Then the amplifier lo signal could be connected to the panel to sense the panel ground. See note 5.030.

8.240 LOW LEVEL INPUTS (GAIN GREATER THAN 10)

8.241 With low level inputs, it is important to operate differentially and to keep both inputs balanced.

8.242 Shielded twisted pairs with equal resistance and capacitive filtering will minimize noise. However, care must be taken to minimize thermal voltages developed due to connectors in each signal path.

8.243 If the signals pass through a connector, they should be routed through adjacent pins to minimize temperature differences of the contacts.

8.244 Additionally, great care must be taken when selecting the resistors in the input filter. Precision metal film resistors can generate a thermoelectric voltage due to the metal film and copper leads. Generally, Allen Bradley carbon composition resistors have a low thermal voltage.

9.000 TROUBLESHOOTING GUIDE

9.010 Before calling the factory with a problem, the following items should be checked:

9.011 The board should be checked in the factory shipped configuration with the factory shipped diagnostic.

9.020 Make sure the address and vector are set to the proper locations.

9.030 The +5 volt supply must be between +4.75 and +5.25 volts.

9.040 All jumper straps are in the proper locations.

9.050 All cables are connected properly (note pin 1 position).

9.060 No components are making contact to an adjacent card.

9.200 SYMPTOMS AND SOLUTIONS

9.210 NO BOARD RESPONSE

9.211 Check steps 9.010 through 9.060

9.212 Clean board connector fingers with a soft pencil eraser.

9.220 DIGITAL OUTPUT CODE IN PLUS OR MINUS FULL SCALE STOPS

9.221 Check for floating inputs per 8.211.

9.222 Check for floating inputs per 5.021.

9.223 Make sure that the input is not greater than the range that the A/D is on.

9.224 Make sure that none of the other inputs is above the plus and minus power supplies. (±15 volts or ±12 volts on/12 models).

9.230 FIRST READING ON A CHANNEL IS INCORRECT

9.231 Settling time problems due to source impedance over 1 kilohm, or CT not installed for higher gains.

9.232 Note step 8.100.

9.233 Input settling time is budgeted from one linear region to another. If the sample and hold is saturated due to overvoltage on an open channel, the first reading on a valid channel could be in error.

9.240 ZERO WILL NOT CALIBRATE

9.241 The total adjustment range of the zero adjust potentiometer is approximately 50 LSB'S. If there are offsets in the system, such as bridge imbalances, they cannot usually be removed with the A/D zero control.

9.242 Check for the floating input per 5.021.

9.245 With high gains, offsets in the signal path due to thermal voltages can cause zero error that cannot be adjusted out. Note steps 8.240.

9.250 FULL SCALE WILL NOT CALIBRATE

9.251 The total adjustment range of the A/D converter range potentiometer is approximately 50 LSB'S. If there are other gain errors in the system, they cannot usually be adjusted out with the A/D converter potentiometer.

9.252 On resistor programmable gain models, the resistor must have an absolute tolerance of ±.02% or the range potentiometer may not calibrate.

9.260 EXCESSIVE NOISE

9.261 Note 8.010.

NEW DIAGNOSTICS POLICY

The Data Translation diagnostics policy may be different from that outlined in your user manual.

Under the new policy, diagnostics must be ordered separately. In addition, the diagnostics for all boards are organized into eight software products, as listed below. The listings of the diagnostics (as opposed to the software products) are included in the hardware user manuals which are shipped with all Data Translation boards.

Data Translation diagnostics are available according to the following scheme.

DATA TRANSLATION DIAGNOSTICS PRODUCTS

1. SP161-CB: paper tape diagnostics package for all STD bus boards (DT2715, DT2722, DT2724, DT2725, DT2726, DT2727, DT2734, DT2735, DT2742, DT2744, and DT2745).

2. SP162-CB: paper tape diagnostics package for the DT1741, DT1742, DT1744, DT1748, DT1751, DT1753, DT1755, DT1759, DT1841, DT1842, and DT1843 MULTIBUS boards.

3. SP163-CB: paper tape diagnostics package for the DT711, DT732, DT724, and DT728 MULTIBUS boards.

4. SP164-CB: paper tape diagnostics package for all Computer Automation boards (DT1731, DT1732, DT1733, DT1734, DT1735, DT1738, and DT1739).

5. SP165-CB: paper tape diagnostics package for all UNIBUS boards.

6. SP165-CY: diagnostics package for all UNIBUS boards, on a single RX01 compatible floppy disk.

7. SP166-CB: paper tape diagnostics package for the LSI-11 quad and dual size boards.

8. SP167-CY: diagnostics package for all LSI-11 compatible boards (including the advanced architecture series) on a single RX01 compatible floppy disk.

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